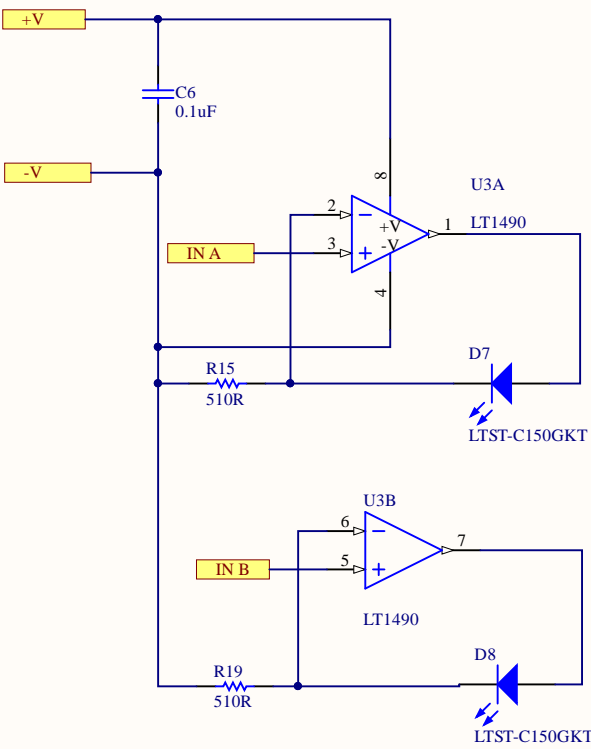
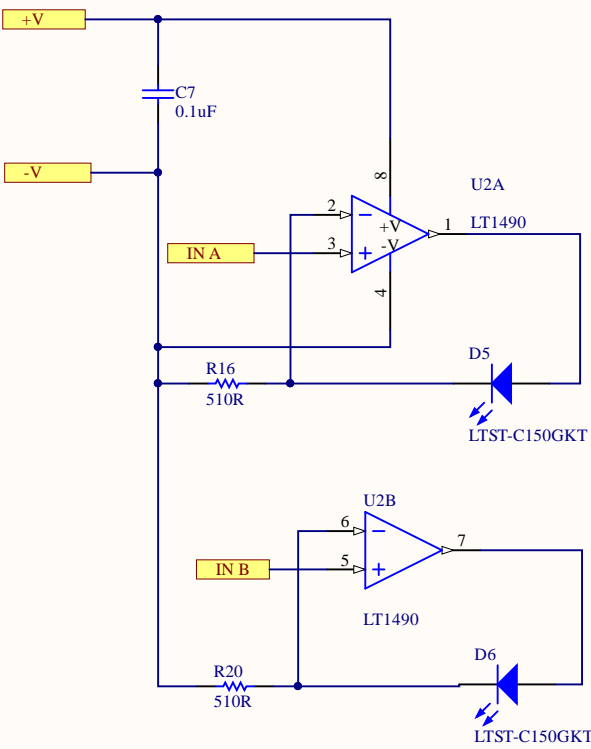
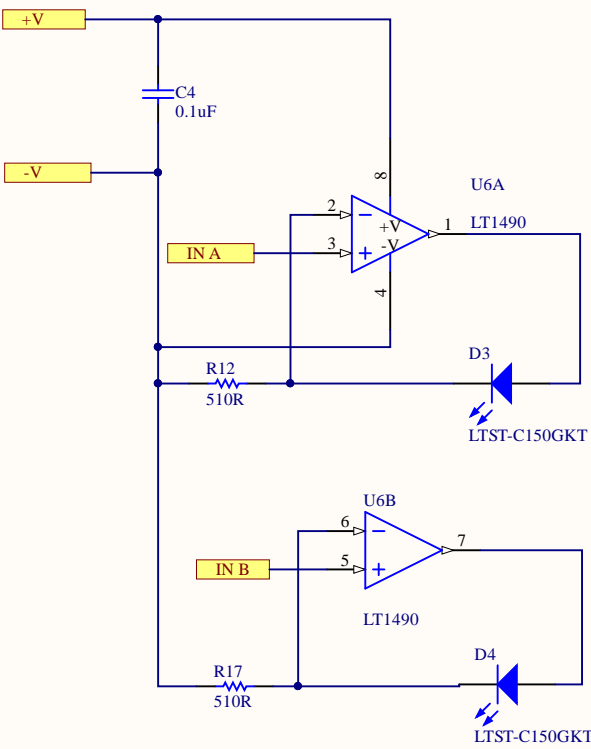
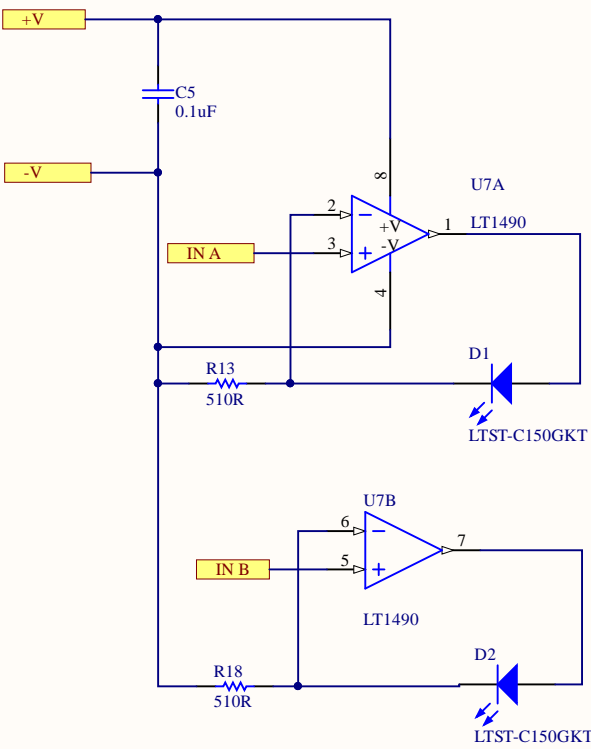


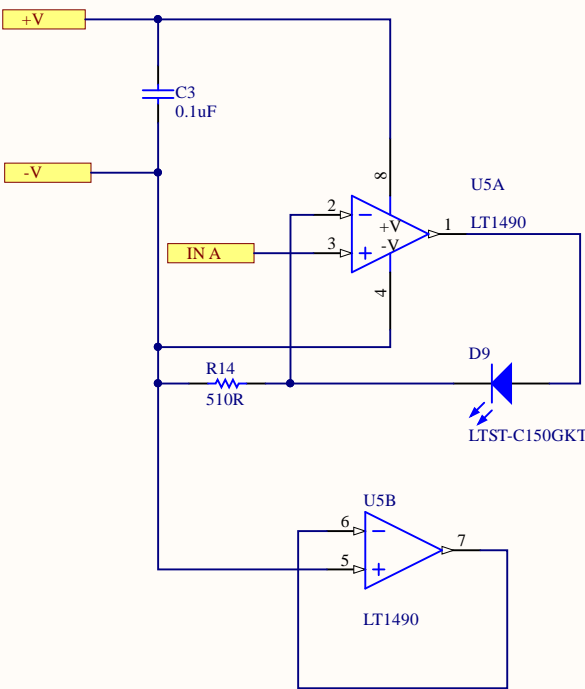
<b>NAVSEA</b> Land Based Engineering Site	ENGINEER:	TITLE:	
	PCB DESIGNER:		
NSWCPD Building 77H Code 514 901 Admiral Peary Way Philadelphia, PA 19112	DATE: 12/18/2018	PART NO.:	REV:
	FILE NAME: ns18257 PXI 2727.PcbDoc	DWG NO.:	SCALE:

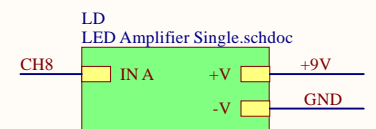
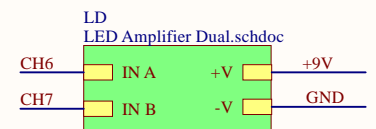
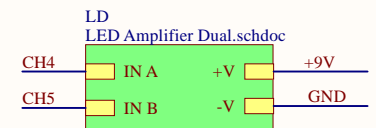
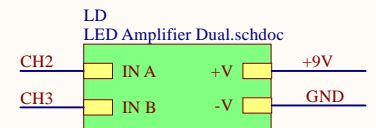
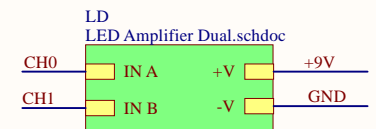
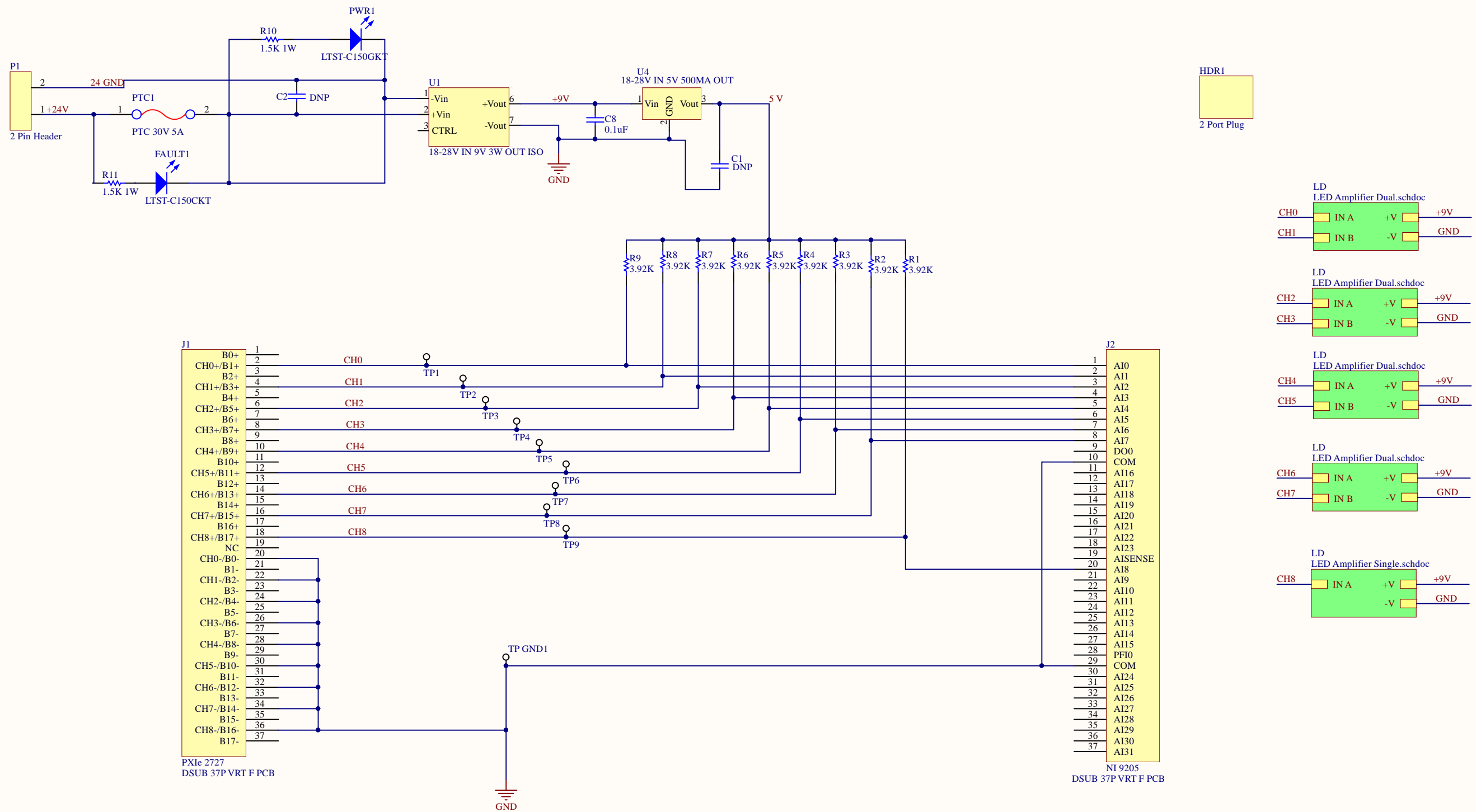


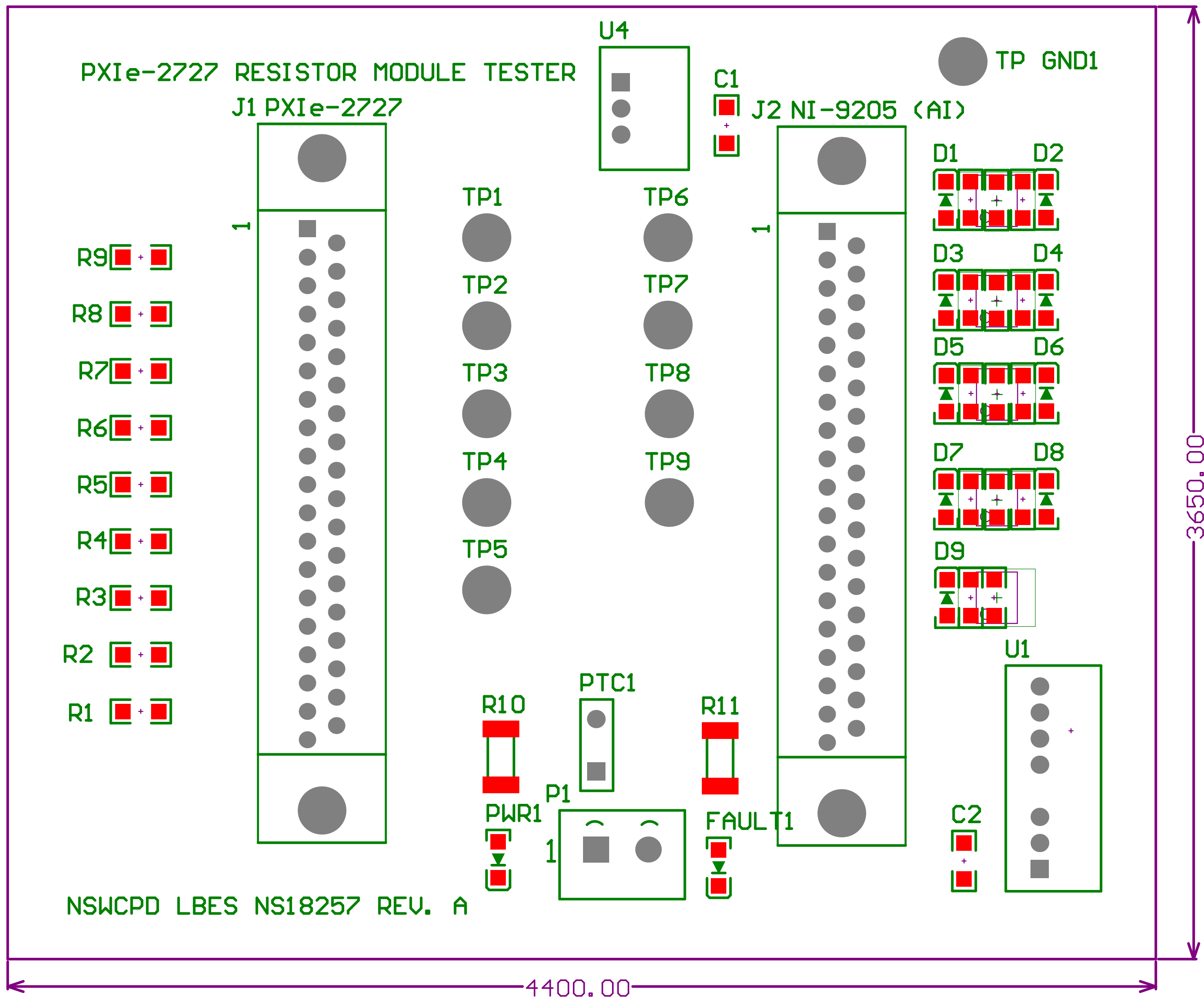






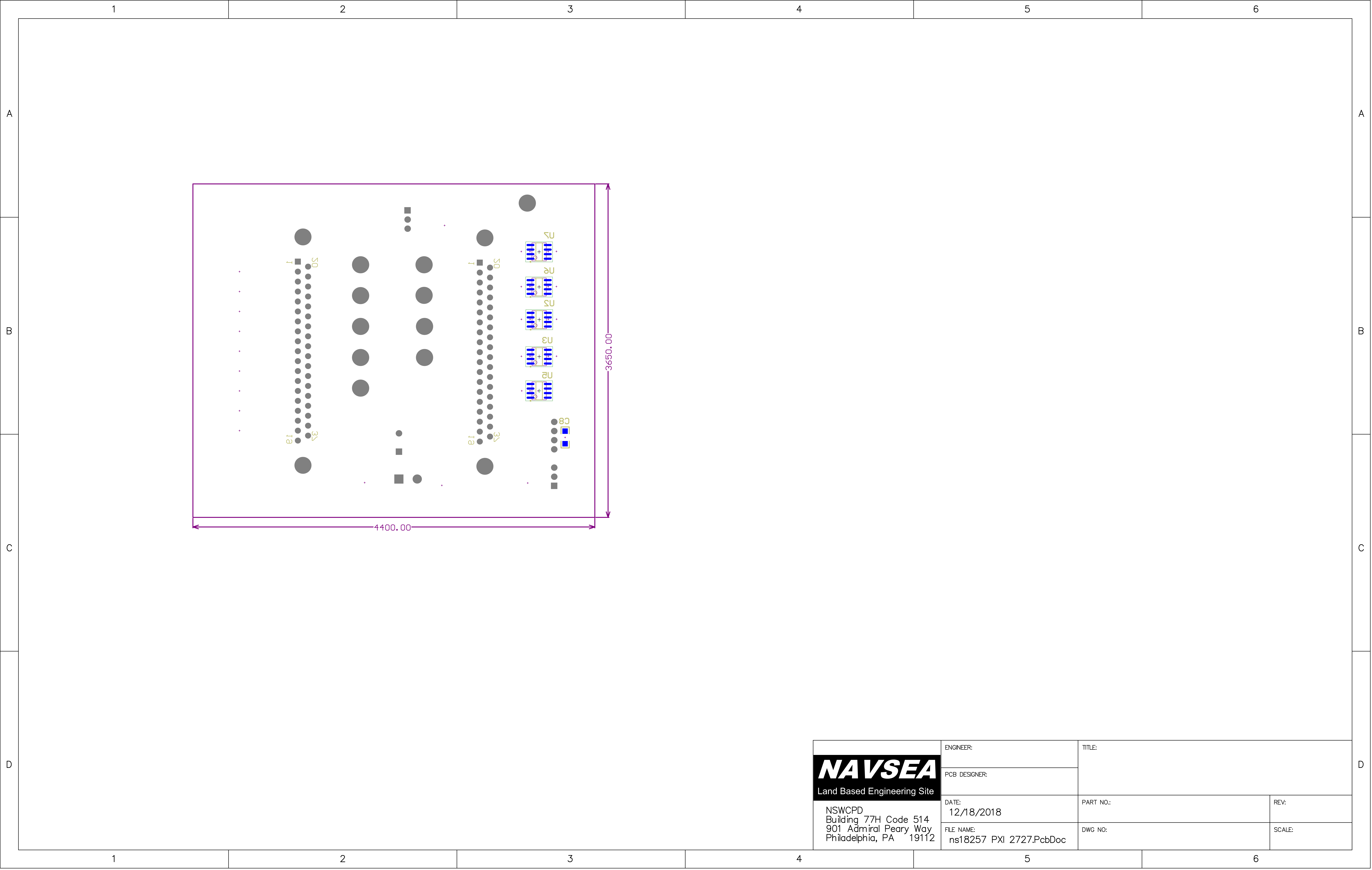






















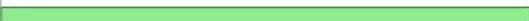
<b>NAVSEA</b> Land Based Engineering Site	ENGINEER:	TITLE:	
	PCB DESIGNER:		
NSWCPD Building 77H Code 514 901 Admiral Peary Way Philadelphia, PA 19112	DATE: 12/18/2018	PART NO.:	REV:
	FILE NAME: ns18257 PXI 2727.PcbDoc	DWG NO:	SCALE:



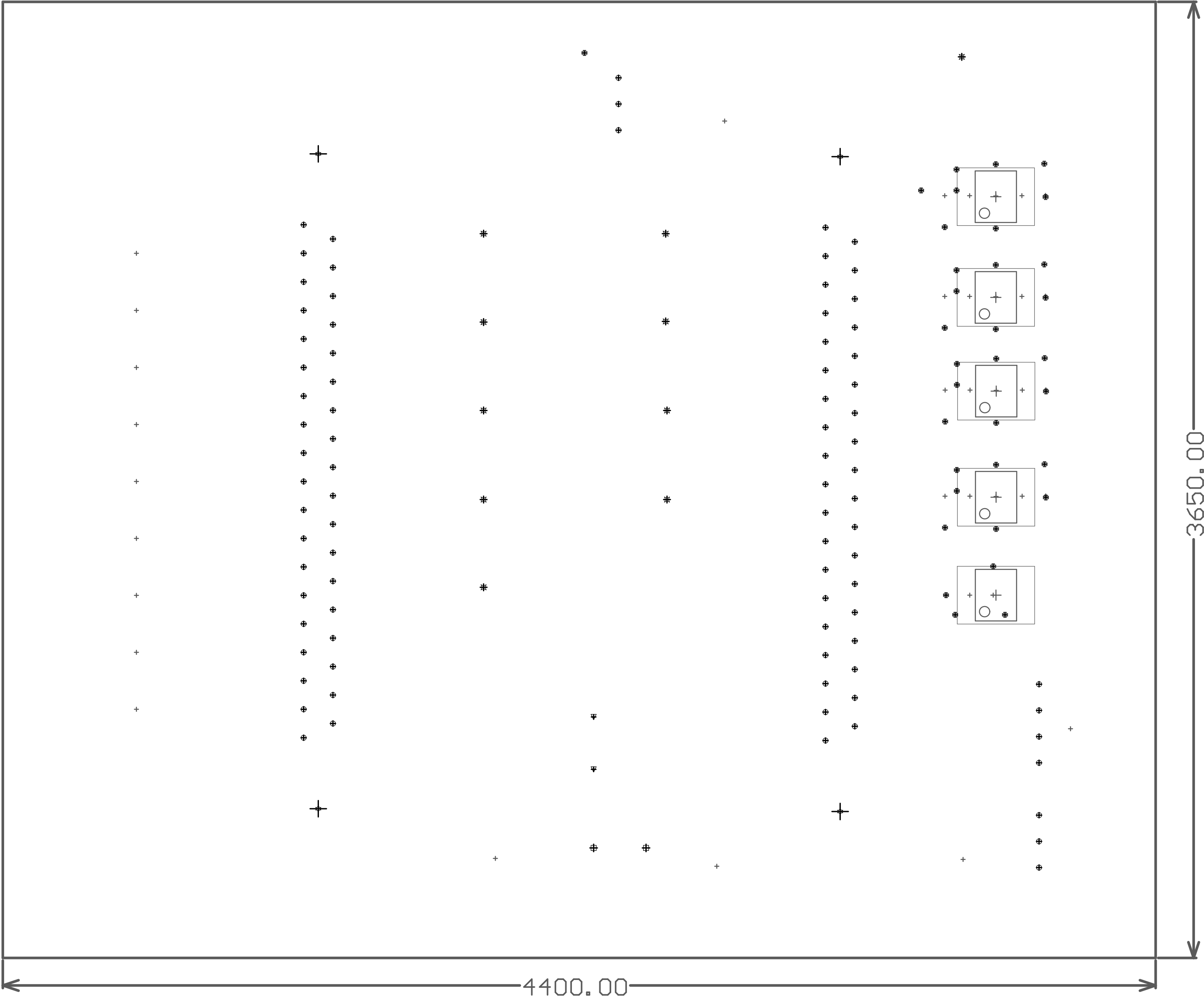


<b>NAVSEA</b> Land Based Engineering Site	ENGINEER:	TITLE:	
	PCB DESIGNER:		
NSWCPD Building 77H Code 514 901 Admiral Peary Way Philadelphia, PA 19112	DATE: 12/18/2018	PART NO.:	REV:
	FILE NAME: ns18257 PXI 2727.PcbDoc	DWG NO:	SCALE:

# Board Stack Report

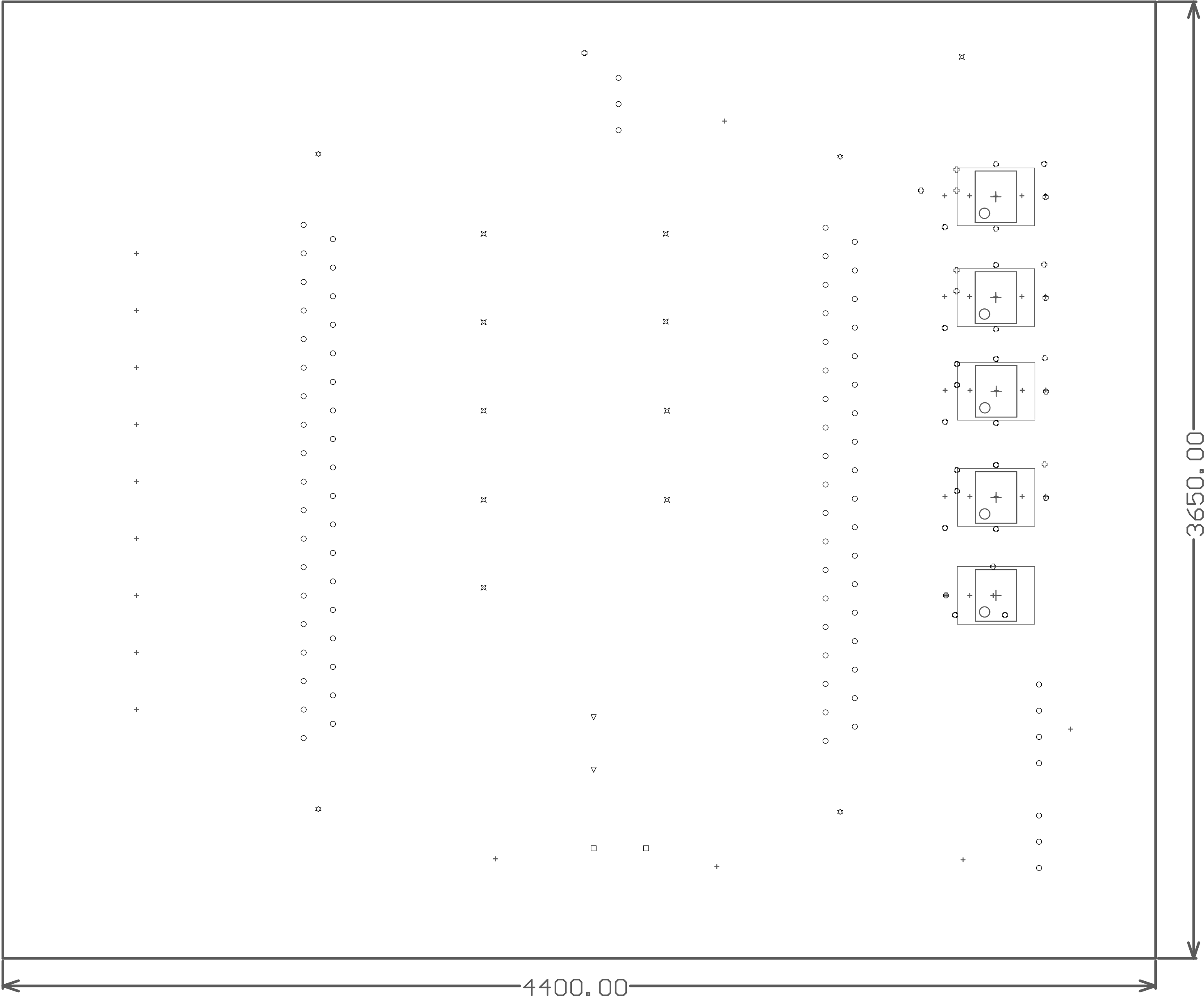
Stack Up		Layer Stack			
Layer	Board Layer Stack	Name	Material	Thickness	Constant
1		Top Paste			
2		Top Overlay			
3	  	Top Solder	Solder Resist	0.40mil	3.5
4	  	Top Layer	Copper	1.40mil	
5		Dielectric1	FR-4	59.00mil	4.8
6	  	Bottom Layer	Copper	1.40mil	
7	  	Bottom Solder	Solder Resist	0.40mil	3.5
8		Bottom Overlay			
9		Bottom Paste			
	Height : 62.60mil				

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Template	Description	Hole Tolerance (+)	Hole Tolerance (-)
▽	2	35.00mil (0.889mm)	PTH	Round	Top Layer - Bottom Layer	Pad	<Mixed>	<Mixed>			
□	2	57.00mil (1.448mm)	PTH	Round	Top Layer - Bottom Layer	Pad	<Mixed>	<Mixed>			
✱	4	125.00mil (3.175mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c470h318			
✕	10	52.00mil (1.321mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c475h132			
⊕	34	14.00mil (0.356mm)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	v71h36			
○	84	40.00mil (1.016mm)	PTH	Round	Top Layer - Bottom Layer	Pad	<Mixed>	<Mixed>			
	136 Total										

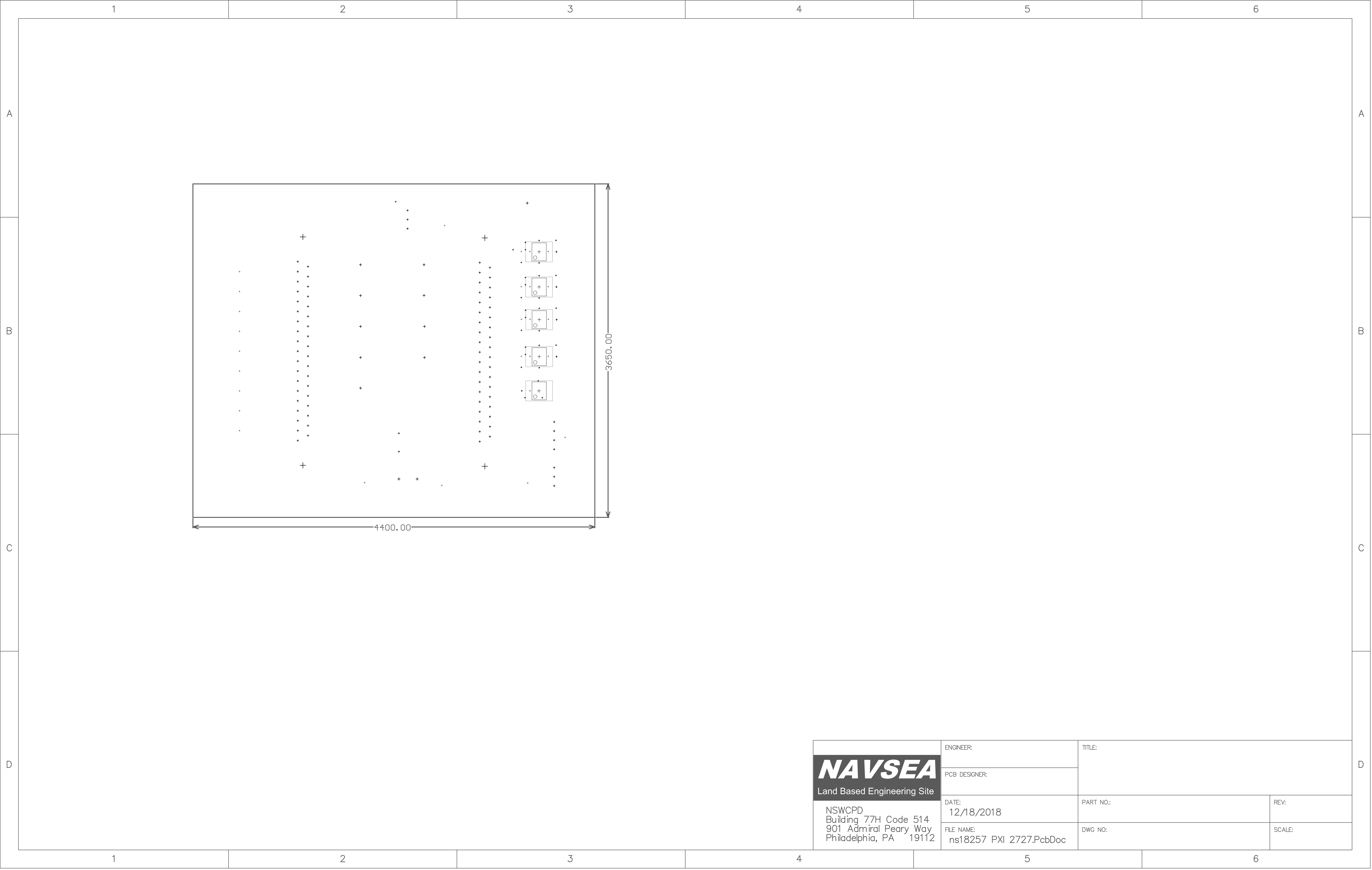


<b>NAVSEA</b> Land Based Engineering Site	ENGINEER:	TITLE:	
	PCB DESIGNER:		
NSWCPD Building 77H Code 514 901 Admiral Peary Way Philadelphia, PA 19112	DATE: 12/18/2018	PART NO.:	REV:
	FILE NAME: ns18257 PXI 2727.PcbDoc	DWG NO:	SCALE:

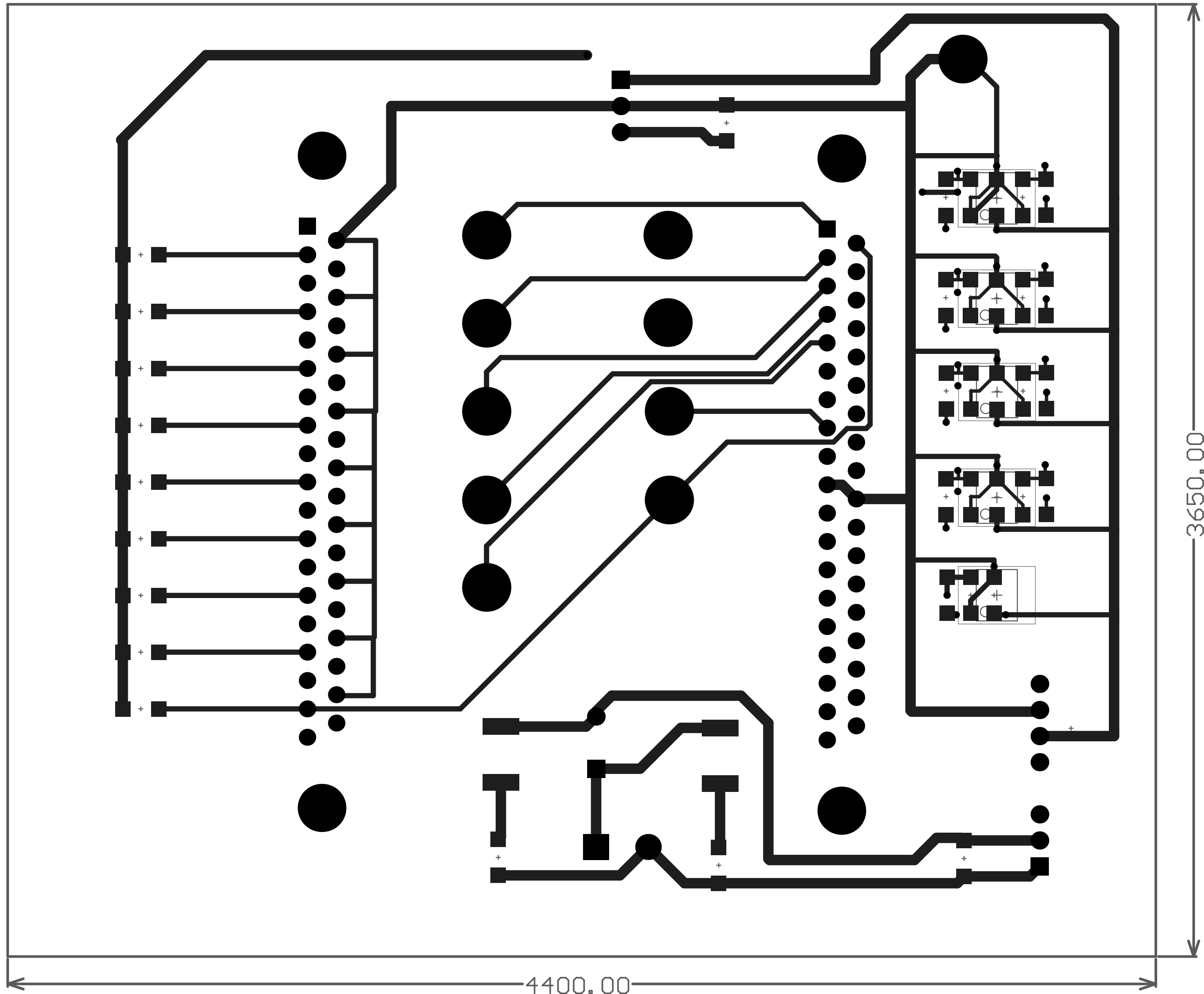
Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Template	Description	Hole Tolerance (+)	Hole Tolerance (-)
▽	2	35.00mil (0.889mm)	PTH	Round	Top Layer - Bottom Layer	Pad	<Mixed>	<Mixed>			
□	2	57.00mil (1.448mm)	PTH	Round	Top Layer - Bottom Layer	Pad	<Mixed>	<Mixed>			
✱	4	125.00mil (3.175mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c470h318			
✱	10	52.00mil (1.321mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c475h132			
⊕	34	14.00mil (0.356mm)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	v71h36			
○	84	40.00mil (1.016mm)	PTH	Round	Top Layer - Bottom Layer	Pad	<Mixed>	<Mixed>			
	136 Total										



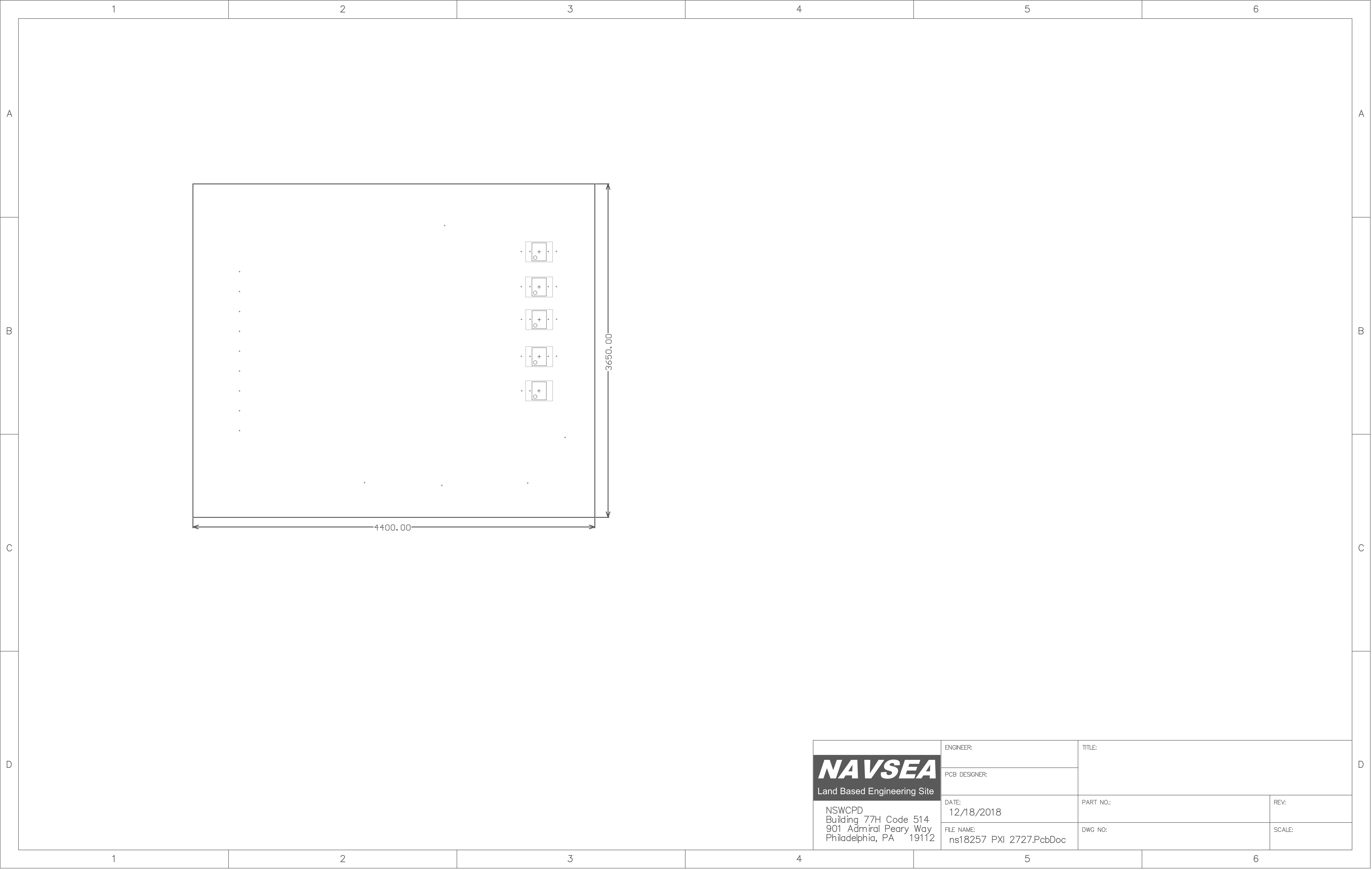
<div>NAVSEA</div> <div>Land Based Engineering Site</div>	ENGINEER:	TITLE:		
	PCB DESIGNER:			
NSWCPD Building 77H Code 514 901 Admiral Peary Way Philadelphia, PA 19112	DATE: 12/18/2018	PART NO.:	REV:	
	FILE NAME: ns18257 PXI 2727.PcbDoc	DWG NO:	SCALE:	



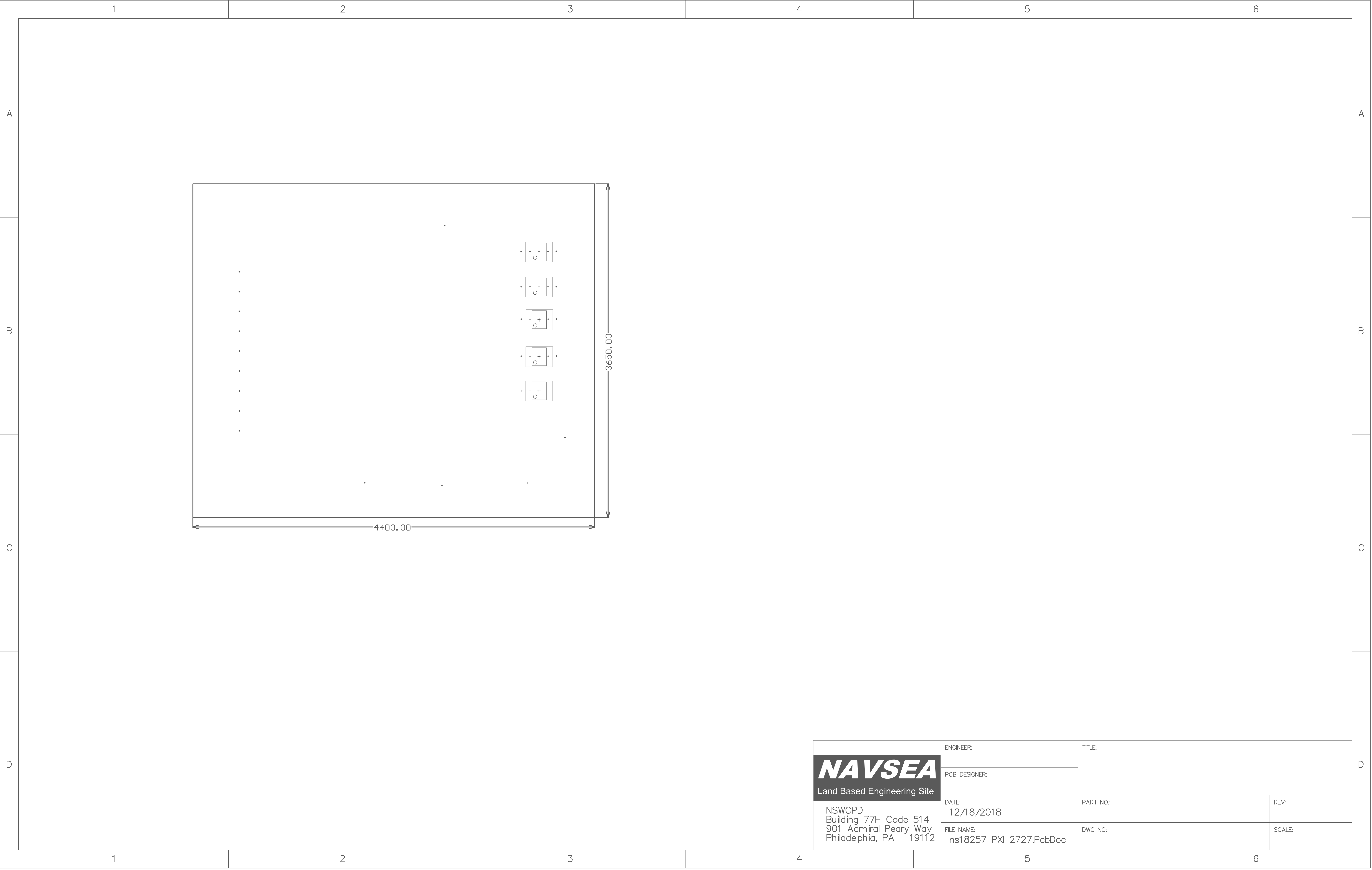
<div>NAVSEA</div> <div>Land Based Engineering Site</div>	ENGINEER:	TITLE:	
	PCB DESIGNER:		
NSWCPD Building 77H Code 514 901 Admiral Peary Way Philadelphia, PA 19112	DATE: 12/18/2018	PART NO.:	REV:
	FILE NAME: ns18257 PXI 2727.PcbDoc	DWG NO:	SCALE:



<div>NAVSEA</div> <div>Land Based Engineering Site</div>	ENGINEER:	TITLE:	
	PCB DESIGNER:		
NSWCPD Building 77H Code 514 901 Admiral Peary Way Philadelphia, PA 19112	DATE: 12/18/2018	PART NO.:	REV:
	FILE NAME: ns18257 PXI 2727.PcbDoc	DWG NO.:	SCALE:

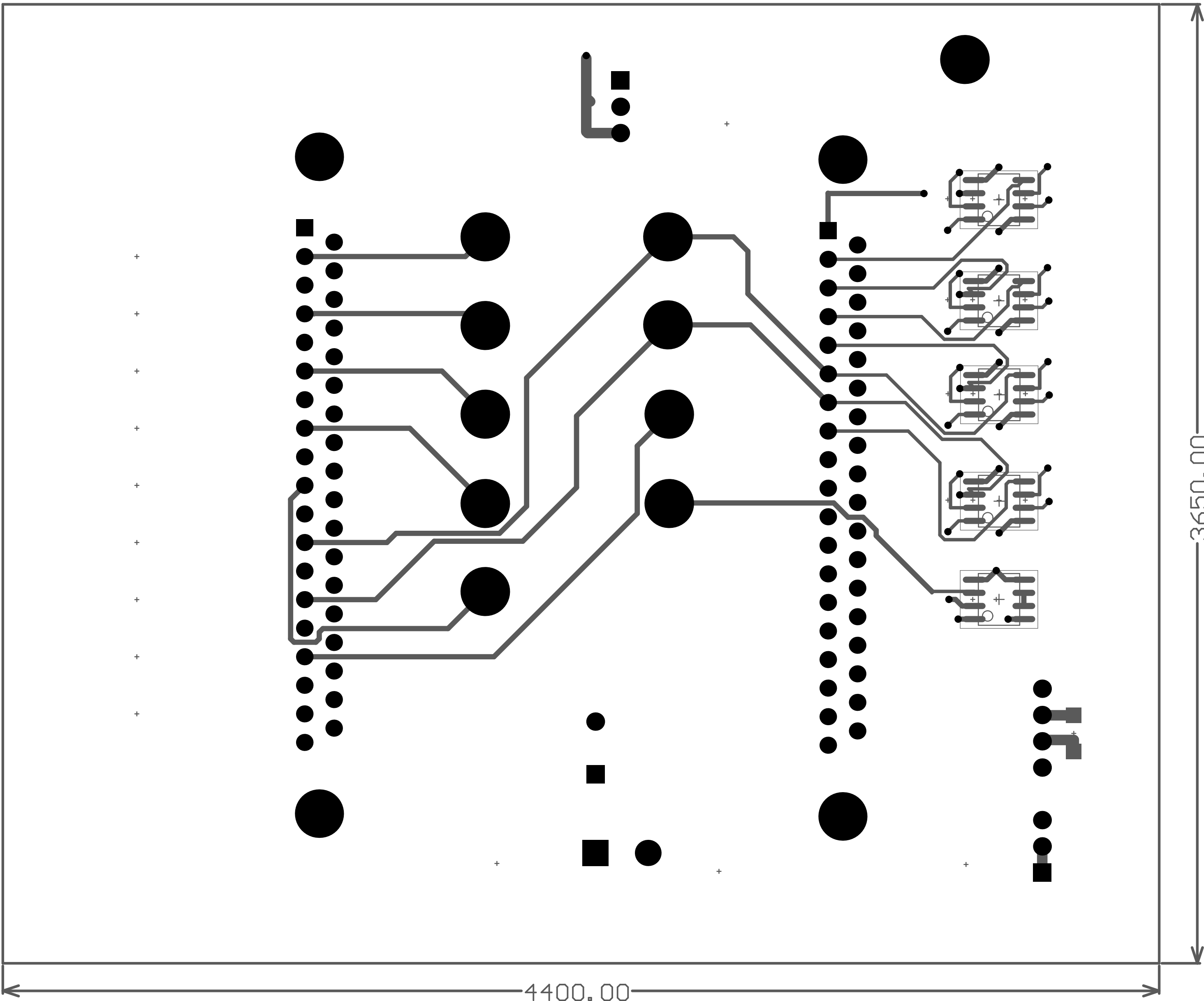


<div>NAVSEA</div> <div>Land Based Engineering Site</div>	ENGINEER:	TITLE:	
	PCB DESIGNER:		
NSWCPD Building 77H Code 514 901 Admiral Peary Way Philadelphia, PA 19112	DATE: 12/18/2018	PART NO.:	REV:
	FILE NAME: ns18257 PXI 2727.PcbDoc	DWG NO:	SCALE:

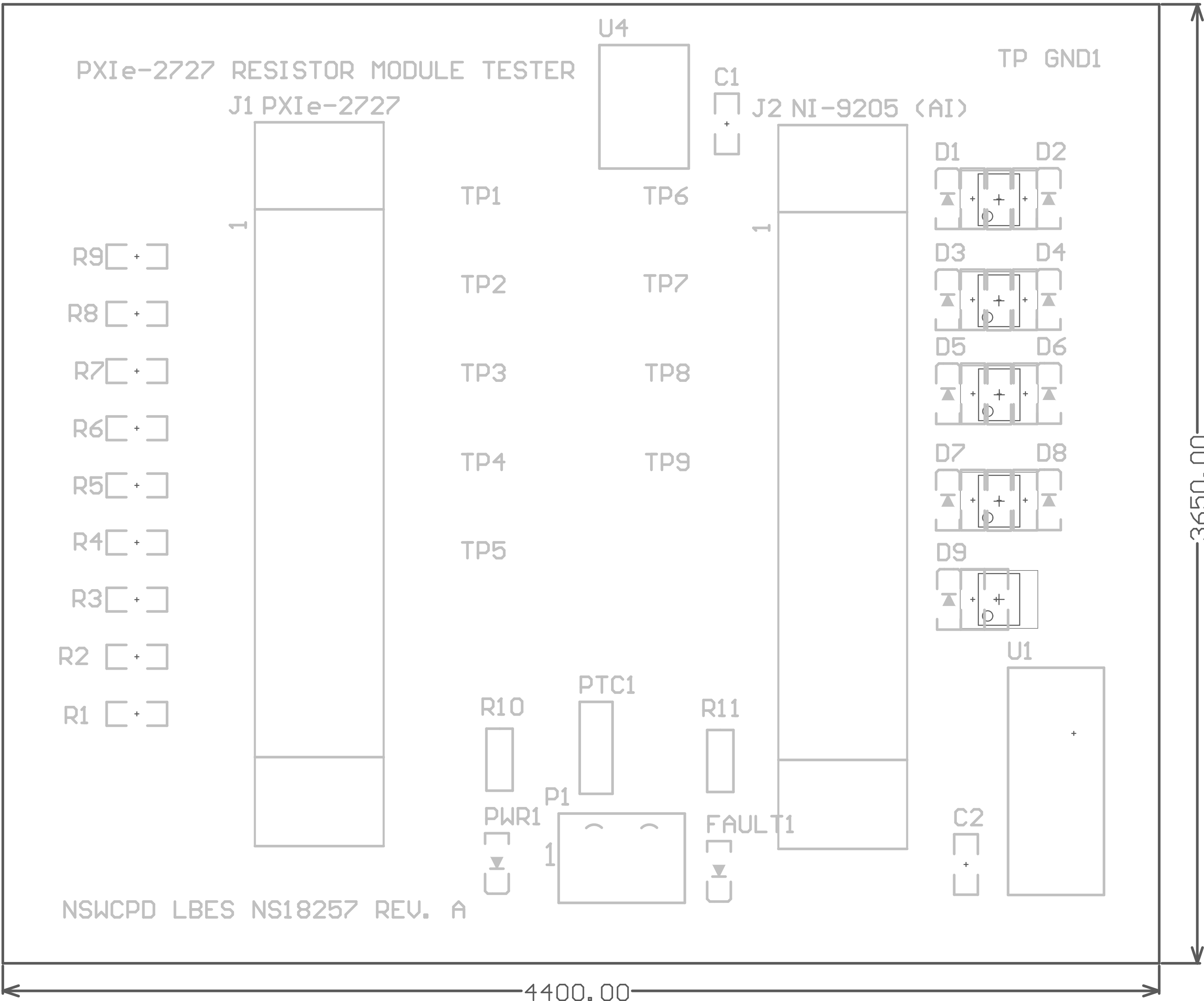


<div>NAVSEA</div> <div>Land Based Engineering Site</div>	ENGINEER:	TITLE:	
	PCB DESIGNER:		
NSWCPD Building 77H Code 514 901 Admiral Peary Way Philadelphia, PA 19112	DATE: 12/18/2018	PART NO.:	REV:
	FILE NAME: ns18257 PXI 2727.PcbDoc	DWG NO:	SCALE:

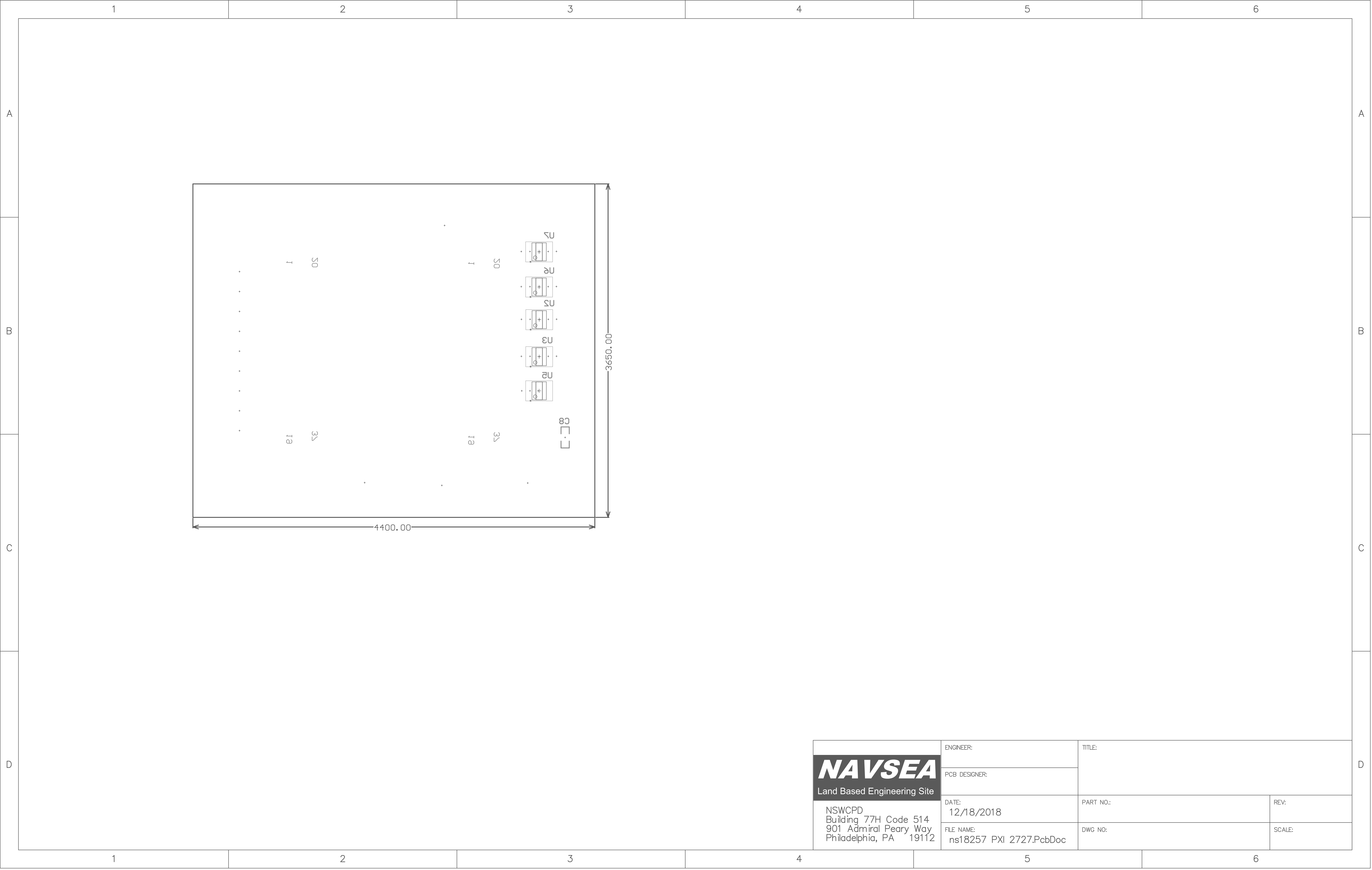




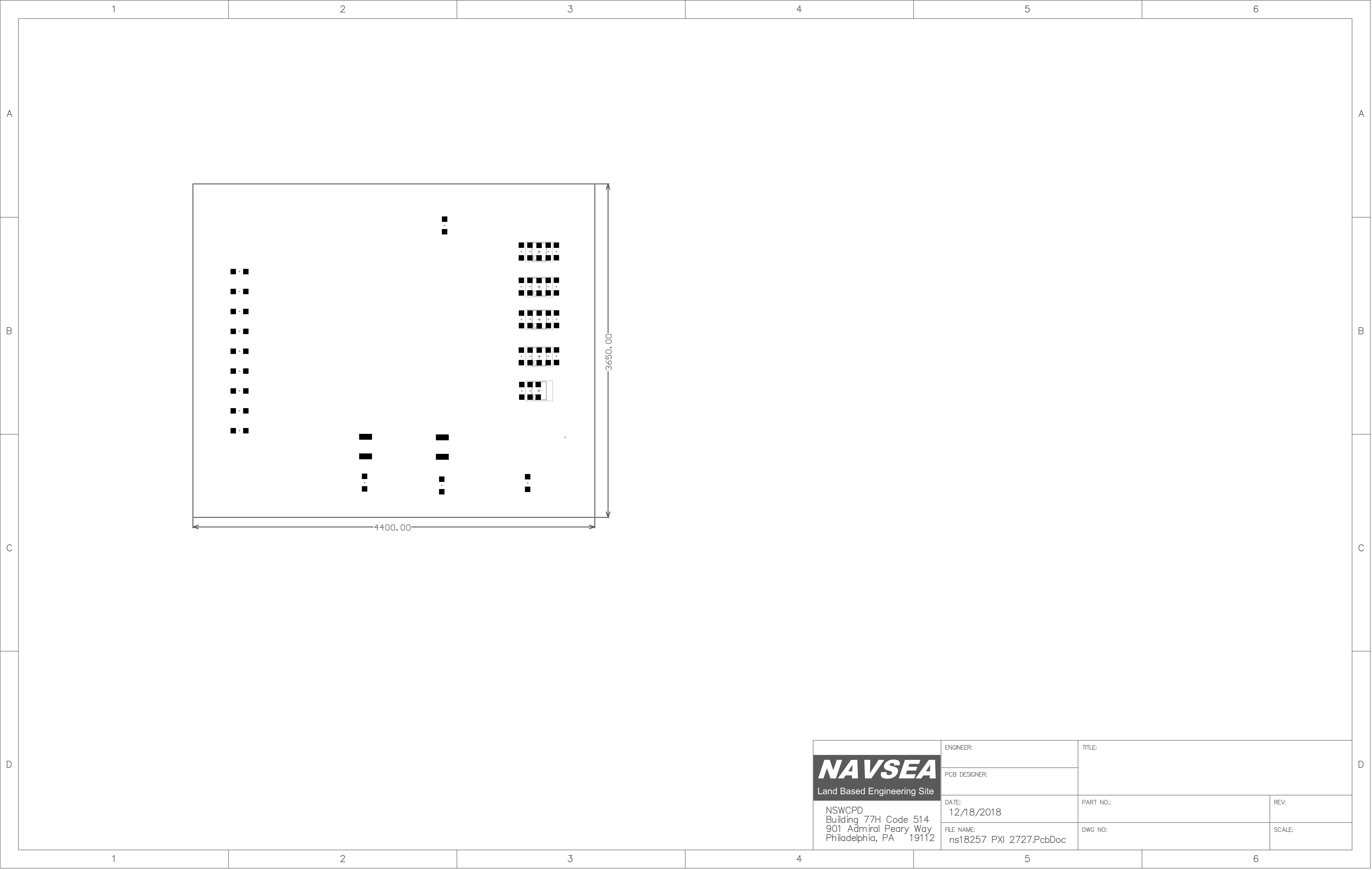
<b>NAVSEA</b> Land Based Engineering Site	ENGINEER:	TITLE:	
	PCB DESIGNER:		
NSWCPD Building 77H Code 514 901 Admiral Peary Way Philadelphia, PA 19112	DATE: 12/18/2018	PART NO.:	REV:
	FILE NAME: ns18257 PXI 2727.PcbDoc	DWG NO:	SCALE:



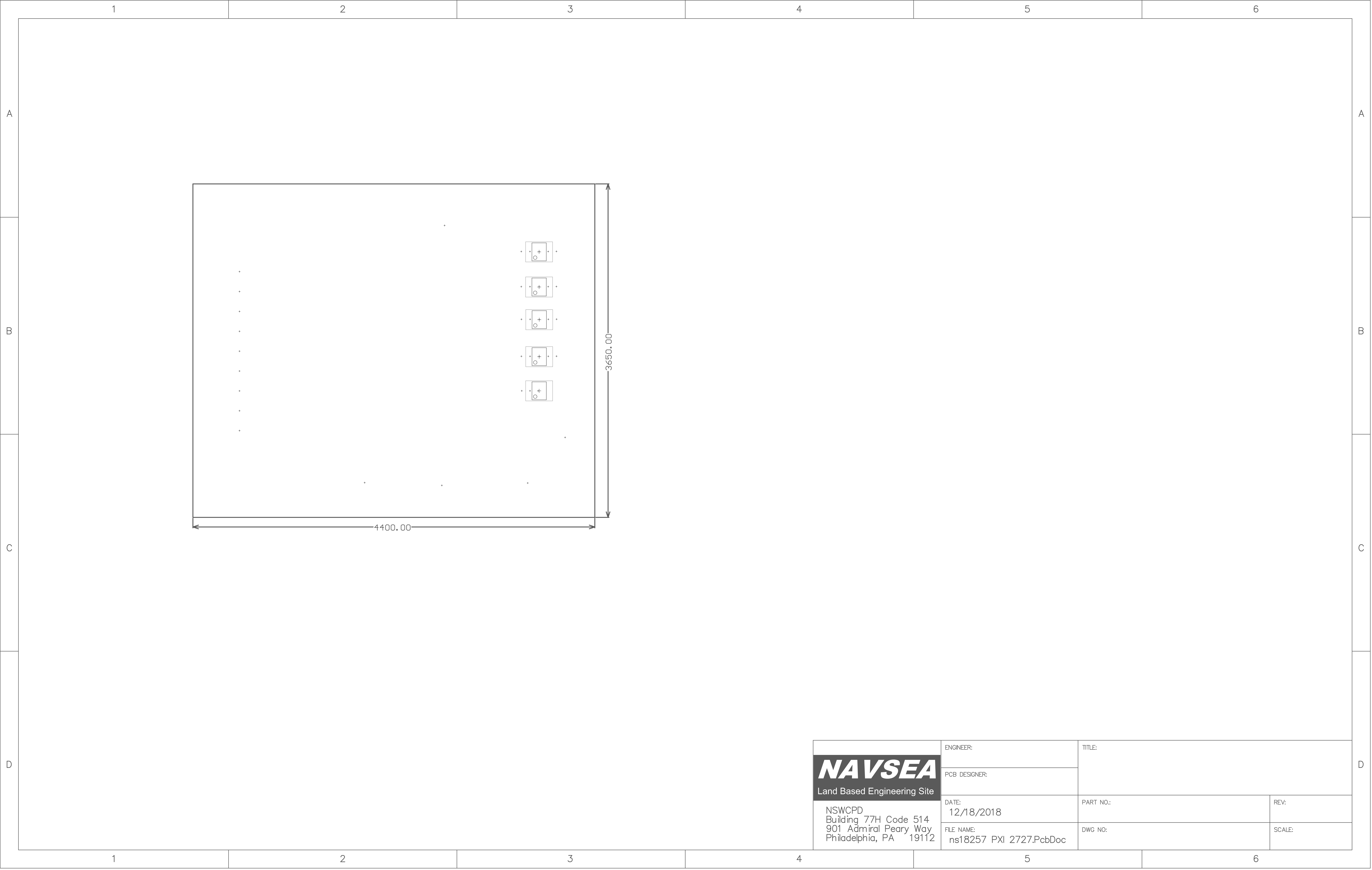
<b>NAVSEA</b> Land Based Engineering Site	ENGINEER:	TITLE:	
	PCB DESIGNER:		
NSWCPD Building 77H Code 514 901 Admiral Peary Way Philadelphia, PA 19112	DATE: 12/18/2018	PART NO.:	REV:
	FILE NAME: ns18257 PXI 2727.PcbDoc	DWG NO:	SCALE:



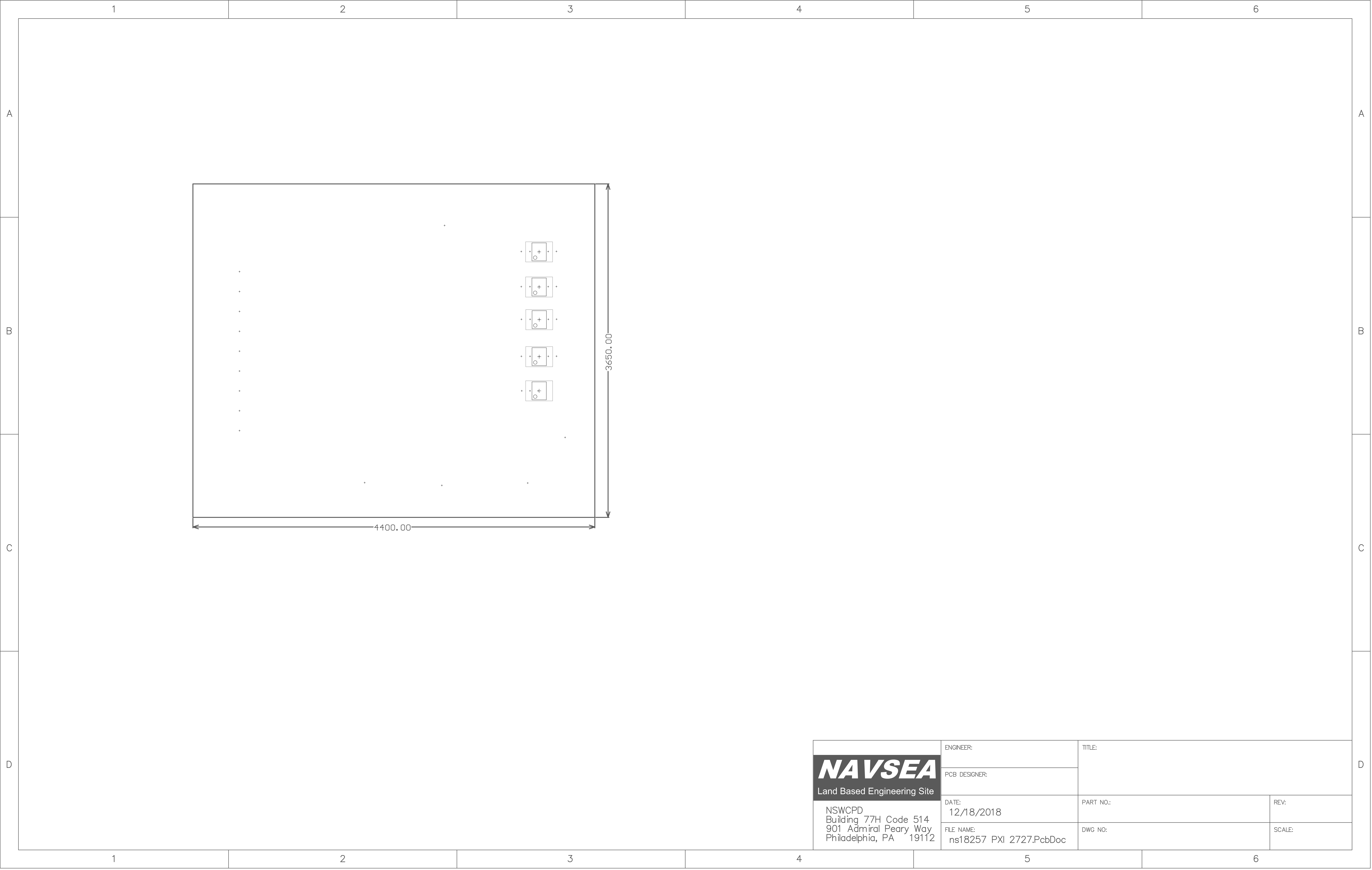
<div>NAVSEA</div> <div>Land Based Engineering Site</div> <div>NSWCPD Building 77H Code 514 901 Admiral Peary Way Philadelphia, PA 19112</div>	ENGINEER:	TITLE:	
	PCB DESIGNER:		
	DATE: 12/18/2018	PART NO.:	REV:
	FILE NAME: ns18257 PXI 2727.PcbDoc	DWG NO.:	SCALE:



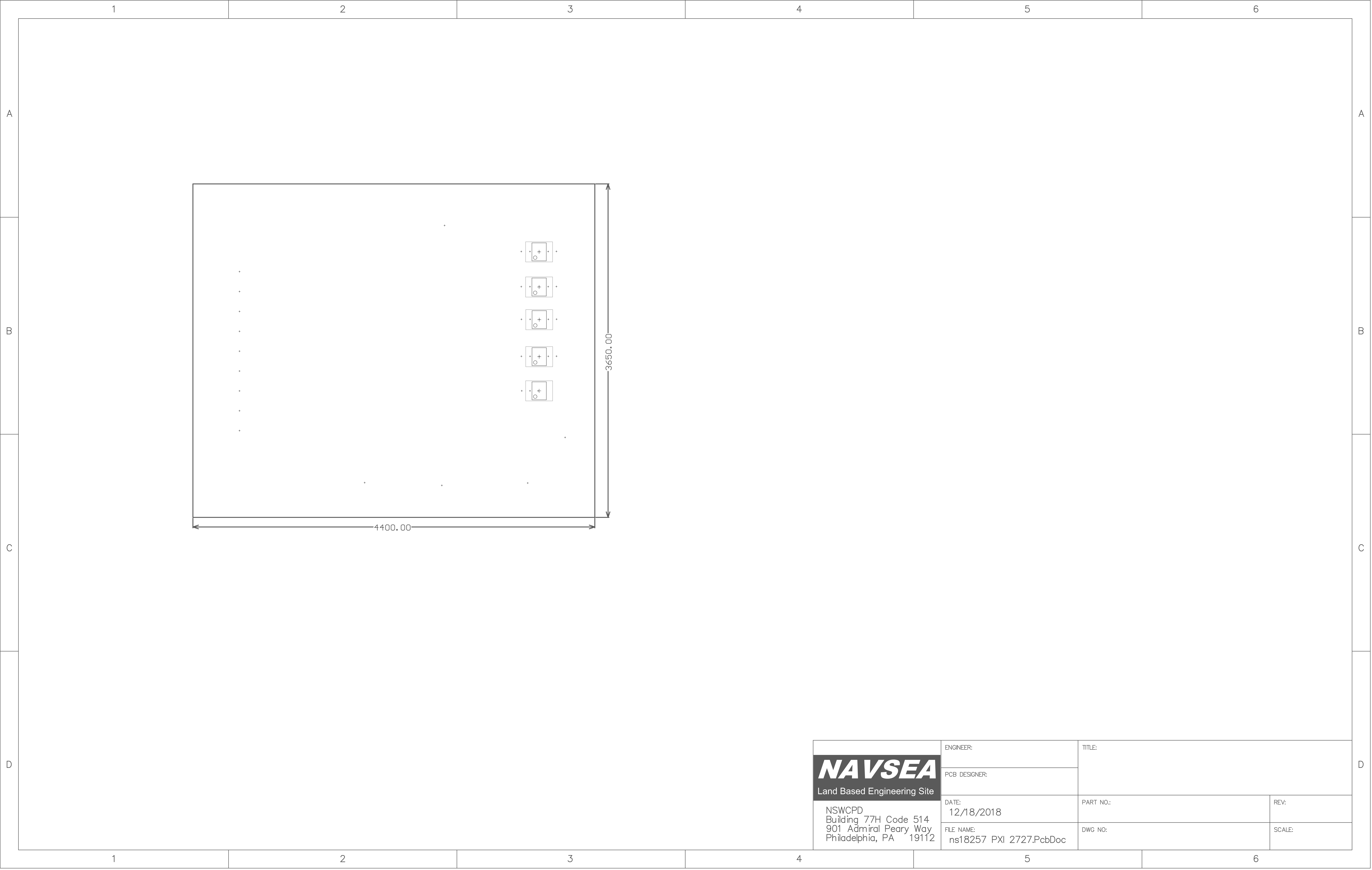
<div>NAVSEA</div> <div>Land Based Engineering Site</div>	ENGINEER:	TITLE:	
	PCB DESIGNER:		
NSWCPD Building 77H Code 514 901 Admiral Peary Way Philadelphia, PA 19112	DATE: 12/18/2018	PART NO.:	REV:
	FILE NAME: ns18257 PXI 2727.PcbDoc	DWG NO:	SCALE:



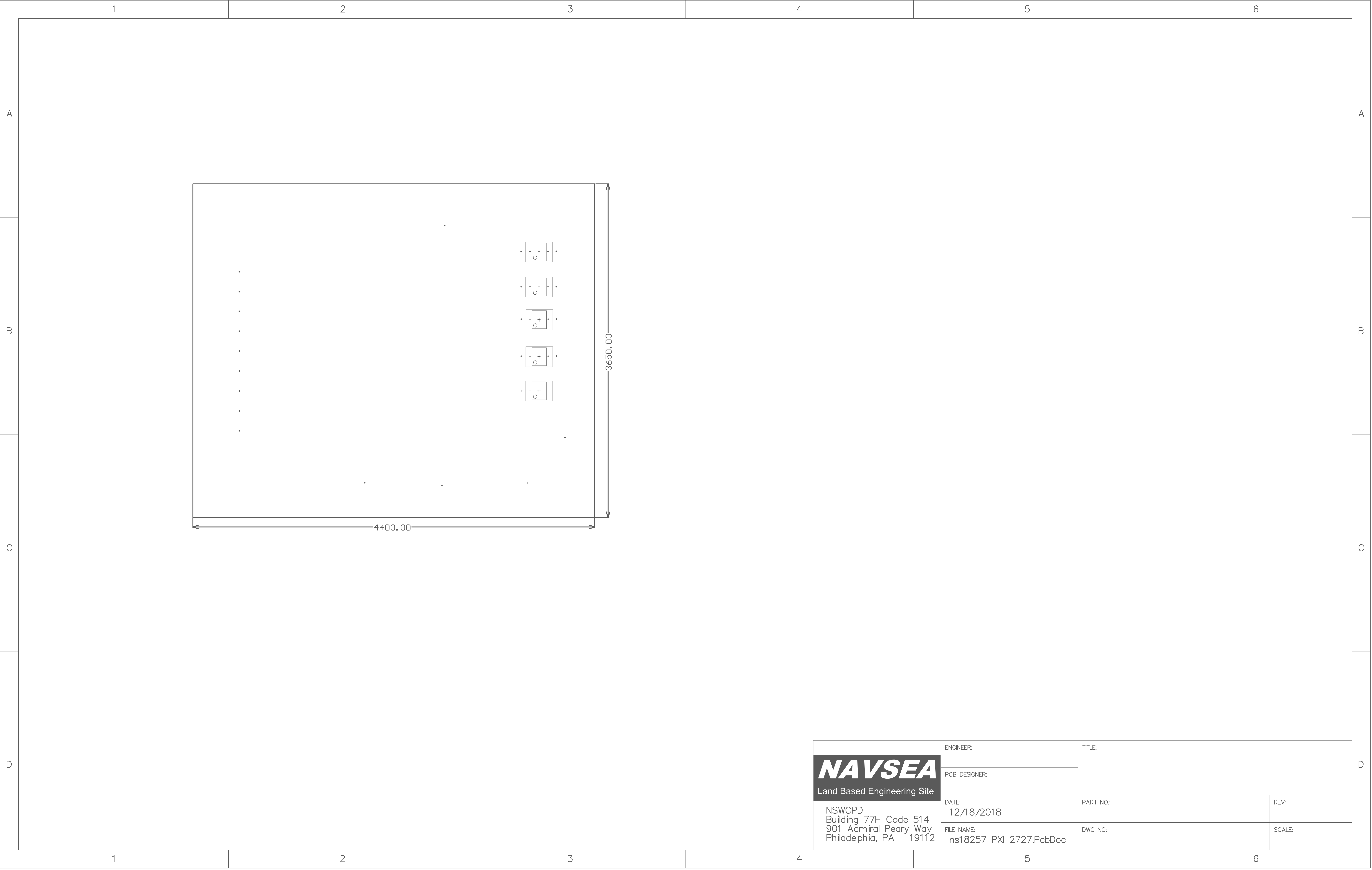
<div>NAVSEA</div> <div>Land Based Engineering Site</div>	ENGINEER:	TITLE:	
	PCB DESIGNER:		
NSWCPD Building 77H Code 514 901 Admiral Peary Way Philadelphia, PA 19112	DATE: 12/18/2018	PART NO.:	REV:
	FILE NAME: ns18257 PXI 2727.PcbDoc	DWG NO:	SCALE:



<div>NAVSEA</div> <div>Land Based Engineering Site</div>	ENGINEER:	TITLE:	
	PCB DESIGNER:		
NSWCPD Building 77H Code 514 901 Admiral Peary Way Philadelphia, PA 19112	DATE: 12/18/2018	PART NO.:	REV:
	FILE NAME: ns18257 PXI 2727.PcbDoc	DWG NO:	SCALE:



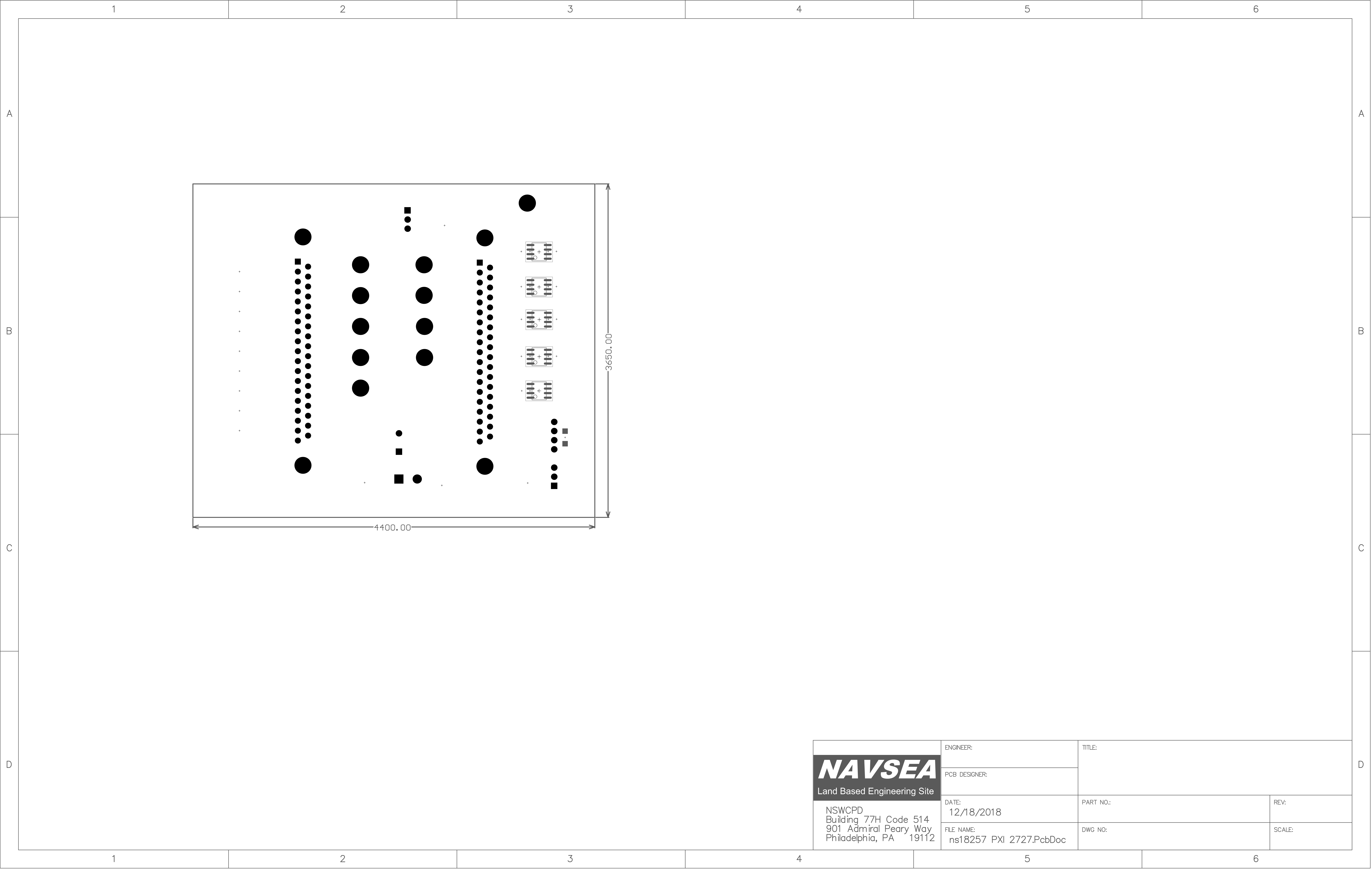
<div>NAVSEA</div> <div>Land Based Engineering Site</div>	ENGINEER:	TITLE:	
	PCB DESIGNER:		
NSWCPD Building 77H Code 514 901 Admiral Peary Way Philadelphia, PA 19112	DATE: 12/18/2018	PART NO.:	REV:
	FILE NAME: ns18257 PXI 2727.PcbDoc	DWG NO:	SCALE:



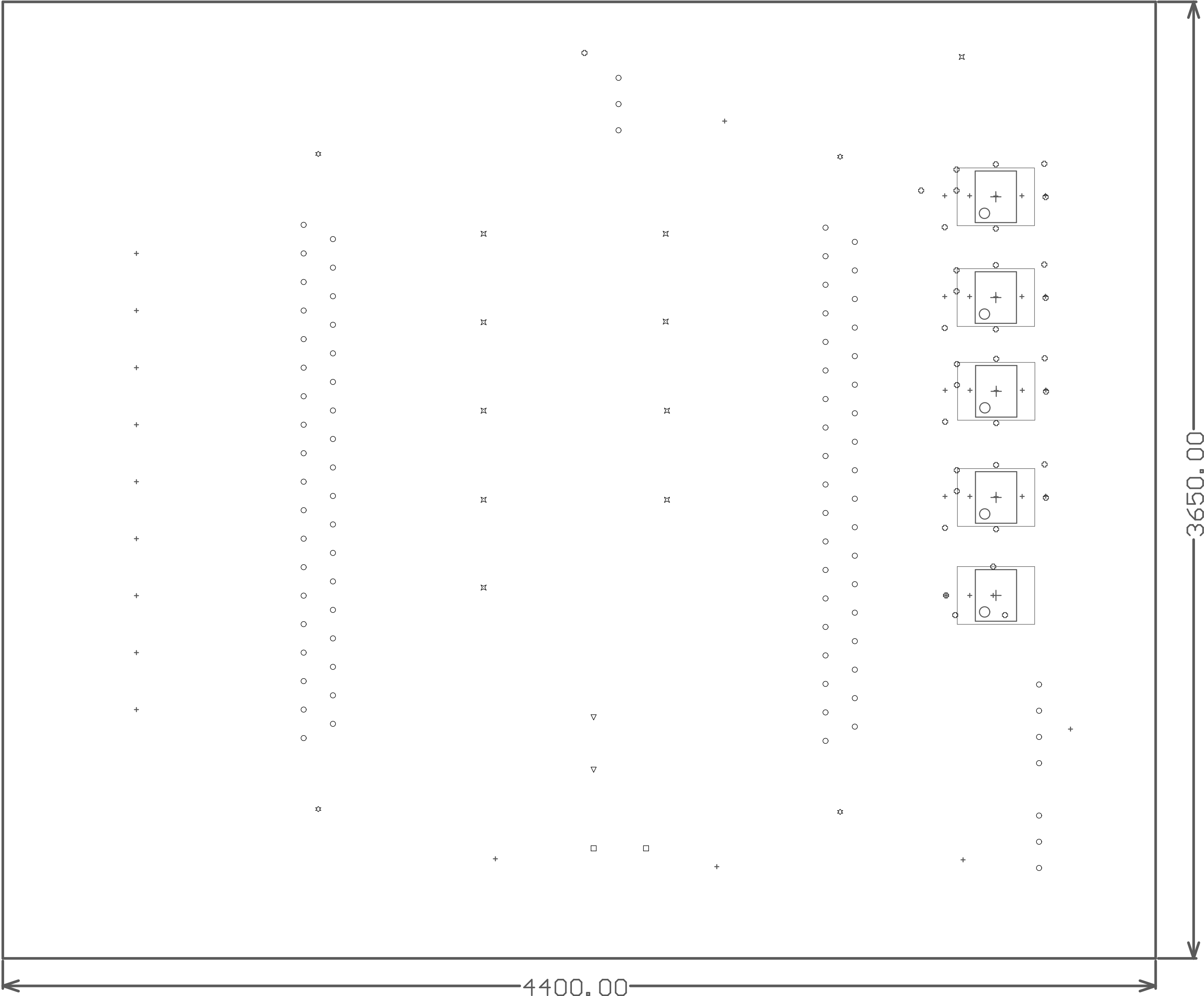
<div>NAVSEA</div> <div>Land Based Engineering Site</div>	ENGINEER:	TITLE:	
	PCB DESIGNER:		
NSWCPD Building 77H Code 514 901 Admiral Peary Way Philadelphia, PA 19112	DATE: 12/18/2018	PART NO.:	REV:
	FILE NAME: ns18257 PXI 2727.PcbDoc	DWG NO:	SCALE:



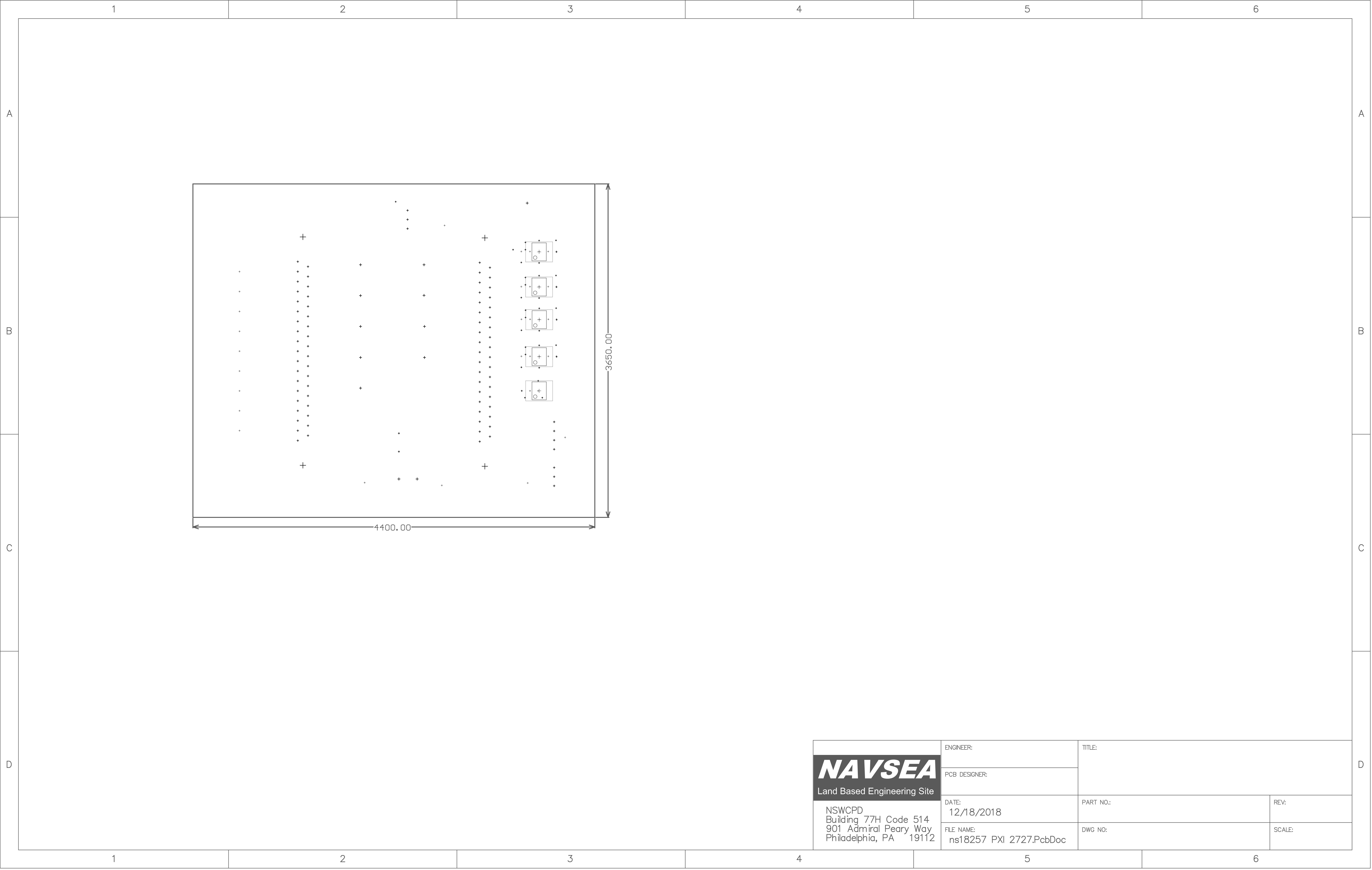




Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Template	Description	Hole Tolerance (+)	Hole Tolerance (-)
▽	2	35.00mil (0.889mm)	PTH	Round	Top Layer - Bottom Layer	Pad	<Mixed>	<Mixed>			
□	2	57.00mil (1.448mm)	PTH	Round	Top Layer - Bottom Layer	Pad	<Mixed>	<Mixed>			
✱	4	125.00mil (3.175mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c470h318			
✱	10	52.00mil (1.321mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c475h132			
⊕	34	14.00mil (0.356mm)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	v71h36			
○	84	40.00mil (1.016mm)	PTH	Round	Top Layer - Bottom Layer	Pad	<Mixed>	<Mixed>			
	136 Total										



<div>NAVSEA</div> <div>Land Based Engineering Site</div>	ENGINEER:	TITLE:		
	PCB DESIGNER:			
NSWCPD Building 77H Code 514 901 Admiral Peary Way Philadelphia, PA 19112	DATE: 12/18/2018	PART NO.:	REV:	
	FILE NAME: ns18257 PXI 2727.PcbDoc	DWG NO:	SCALE:	



<div>NAVSEA</div> <div>Land Based Engineering Site</div>	ENGINEER:	TITLE:	
	PCB DESIGNER:		
NSWCPD Building 77H Code 514 901 Admiral Peary Way Philadelphia, PA 19112	DATE: 12/18/2018	PART NO.:	REV:
	FILE NAME: ns18257 PXI 2727.PcbDoc	DWG NO:	SCALE:

## Design Rules Verification Report

Filename : C:\Users\Public\Documents\Altium\Projects\NS18257 PXIe 2727\ns18257 PXI 272

Warnings 0  
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=10mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ( (All) )	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=13mil) (Max=100mil) (Preferred=20mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Hole Size Constraint (Min=1mil) (Max=270mil) (All)	0
Pads and Vias to follow the Drill pairs settings	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Room LD4 (Bounding Region = (5850mil, 6815mil, 6350mil, 7085mil) (InComponentClass('LD4'))	0
Room LD3 (Bounding Region = (5850mil, 6430.512mil, 6350mil, 6700.512mil) (InComponentClass('LD3'))	0
Room NS18257 PXIe 2727 (Bounding Region = (2690mil, 4255mil, 6515mil, 7590mil) (InComponentClass('NS18257	0
Room LD (Bounding Region = (5850mil, 5295mil, 6260mil, 5555mil) (InComponentClass('LD'))	0
Room LD1 (Bounding Region = (5851.024mil, 5667.795mil, 6351.024mil, 5937.795mil) (InComponentClass('LD1'))	0
Room LD2 (Bounding Region = (5851.535mil, 6072.795mil, 6351.535mil, 6342.795mil) (InComponentClass('LD2'))	0
Total	0

## Electrical Rules Check Report

Class	Document	Message
Warning	LED Amplifier Single.SchDoc	NetC3_1 contains Input Pin and Unspecified Port objects (Pin U5-5,Port -V)
Warning	NS18257 PXIe 2727.SchDoc	Net CH0 has no driving source (Pin J1-2,Pin J2-1,Pin R9-1,Pin TP1-1,Pin U7-3)
Warning	NS18257 PXIe 2727.SchDoc	Net CH1 has no driving source (Pin J1-4,Pin J2-2,Pin R8-1,Pin TP2-1,Pin U7-5)
Warning	NS18257 PXIe 2727.SchDoc	Net CH2 has no driving source (Pin J1-6,Pin J2-3,Pin R7-1,Pin TP3-1,Pin U6-3)
Warning	NS18257 PXIe 2727.SchDoc	Net CH3 has no driving source (Pin J1-8,Pin J2-4,Pin R6-1,Pin TP4-1,Pin U6-5)
Warning	NS18257 PXIe 2727.SchDoc	Net CH4 has no driving source (Pin J1-10,Pin J2-5,Pin R5-1,Pin TP5-1,Pin U2-3)
Warning	NS18257 PXIe 2727.SchDoc	Net CH5 has no driving source (Pin J1-12,Pin J2-6,Pin R4-1,Pin TP6-1,Pin U2-5)
Warning	NS18257 PXIe 2727.SchDoc	Net CH6 has no driving source (Pin J1-14,Pin J2-7,Pin R3-1,Pin TP7-1,Pin U3-3)
Warning	NS18257 PXIe 2727.SchDoc	Net CH7 has no driving source (Pin J1-16,Pin J2-8,Pin R2-1,Pin TP8-1,Pin U3-5)
Warning	NS18257 PXIe 2727.SchDoc	Net CH8 has no driving source (Pin J1-18,Pin J2-20,Pin R1-1,Pin TP9-1,Pin U5-3)
Warning	LED Amplifier Dual.SchDoc	Net NetD1_2 has no driving source (Pin D1-2,Pin R13-2,Pin U7-2)
Warning	LED Amplifier Dual.SchDoc	Net NetD2_2 has no driving source (Pin D2-2,Pin R18-2,Pin U7-6)
Warning	LED Amplifier Dual.SchDoc	Net NetD3_2 has no driving source (Pin D3-2,Pin R12-2,Pin U6-2)
Warning	LED Amplifier Dual.SchDoc	Net NetD4_2 has no driving source (Pin D4-2,Pin R17-2,Pin U6-6)
Warning	LED Amplifier Dual.SchDoc	Net NetD5_2 has no driving source (Pin D5-2,Pin R16-2,Pin U2-2)
Warning	LED Amplifier Dual.SchDoc	Net NetD6_2 has no driving source (Pin D6-2,Pin R20-2,Pin U2-6)
Warning	LED Amplifier Dual.SchDoc	Net NetD7_2 has no driving source (Pin D7-2,Pin R15-2,Pin U3-2)
Warning	LED Amplifier Dual.SchDoc	Net NetD8_2 has no driving source (Pin D8-2,Pin R19-2,Pin U3-6)
Warning	LED Amplifier Single.SchDoc	Net NetD9_2 has no driving source (Pin D9-2,Pin R14-2,Pin U5-2)
Warning	NS18257 PXIe 2727.SchDoc	Nets Wire +9V has multiple names (Net Label +9V,Net Label +9V,Net Label +9V,Net Label +9V,Net Label +9V,Net Label +9V,Sheet Entry LD-+V(Passive),Sheet Entry LD-+V(Passive),Sheet Entry LD-+V(Passive),Sheet Entry LD-+V(Passive),Sheet Entry LD-+V(Passive))
Warning	NS18257 PXIe 2727.SchDoc	Nets Wire +9V has multiple names (Sheet Entry LD-+V(Passive),Sheet Entry LD-+V(Passive),Sheet Entry LD-+V(Passive),Sheet Entry LD-+V(Passive),Sheet Entry LD-+V(Passive),Net Label +9V,Net Label +9V,Net Label +9V,Net Label +9V,Net Label +9V,Net Label +9V)
Warning	NS18257 PXIe 2727.SchDoc	Nets Wire CH0 has multiple names (Net Label CH0,Net Label CH0,Sheet Entry LD-IN A(Passive))
Warning	NS18257 PXIe 2727.SchDoc	Nets Wire CH0 has multiple names (Sheet Entry LD-IN A(Passive),Net Label CH0,Net Label CH0)
Warning	NS18257 PXIe 2727.SchDoc	Nets Wire CH1 has multiple names (Net Label CH1,Net Label CH1,Sheet Entry LD-IN B(Passive))
Warning	NS18257 PXIe 2727.SchDoc	Nets Wire CH1 has multiple names (Sheet Entry LD-IN B(Passive),Net Label CH1,Net Label CH1)
Warning	NS18257 PXIe 2727.SchDoc	Nets Wire CH2 has multiple names (Net Label CH2,Net Label CH2,Sheet Entry LD-IN A(Passive))
Warning	NS18257 PXIe 2727.SchDoc	Nets Wire CH2 has multiple names (Sheet Entry LD-IN A(Passive),Net Label CH2,Net Label CH2)
Warning	NS18257 PXIe 2727.SchDoc	Nets Wire CH3 has multiple names (Net Label CH3,Net Label CH3,Sheet Entry LD-IN B(Passive))
Warning	NS18257 PXIe 2727.SchDoc	Nets Wire CH3 has multiple names (Sheet Entry LD-IN B(Passive),Net Label CH3,Net Label CH3)
Warning	NS18257 PXIe 2727.SchDoc	Nets Wire CH4 has multiple names (Net Label CH4,Net Label CH4,Sheet Entry LD-IN A(Passive))
Warning	NS18257 PXIe 2727.SchDoc	Nets Wire CH4 has multiple names (Sheet Entry LD-IN A(Passive),Net Label CH4,Net Label CH4)
Warning	NS18257 PXIe 2727.SchDoc	Nets Wire CH5 has multiple names (Net Label CH5,Net Label CH5,Sheet Entry LD-IN B(Passive))
Warning	NS18257 PXIe 2727.SchDoc	Nets Wire CH5 has multiple names (Sheet Entry LD-IN B(Passive),Net Label CH5,Net Label CH5)
Warning	NS18257 PXIe 2727.SchDoc	Nets Wire CH6 has multiple names (Net Label CH6,Net Label CH6,Sheet Entry LD-IN A(Passive))
Warning	NS18257 PXIe 2727.SchDoc	Nets Wire CH6 has multiple names (Sheet Entry LD-IN A(Passive),Net Label CH6,Net Label CH6)
Warning	NS18257 PXIe 2727.SchDoc	Nets Wire CH7 has multiple names (Net Label CH7,Net Label CH7,Sheet Entry LD-IN B(Passive))
Warning	NS18257 PXIe 2727.SchDoc	Nets Wire CH7 has multiple names (Sheet Entry LD-IN B(Passive),Net Label CH7,Net Label CH7)
Warning	NS18257 PXIe 2727.SchDoc	Nets Wire CH8 has multiple names (Net Label CH8,Net Label CH8,Sheet Entry LD-IN A(Passive))
Warning	NS18257 PXIe 2727.SchDoc	Nets Wire CH8 has multiple names (Sheet Entry LD-IN A(Passive),Net Label CH8,Net Label CH8)

Class	Document	Message
Warning	NS18257 PXIe 2727.SchDoc	CH8) Nets Wire GND has multiple names (Net Label GND,Net Label GND,Net Label GND,Net Label GND,Net Label GND,Power Object GND,Power Object GND,Sheet Entry LD--V(Passive),Sheet Entry LD--V(Passive),Sheet Entry LD--V(Passive),Sheet Entry LD--V(Passive),Sheet Entry LD--V(Passive))
Warning	NS18257 PXIe 2727.SchDoc	Nets Wire GND has multiple names (Sheet Entry LD--V(Passive),Sheet Entry LD--V(Passive),Sheet Entry LD--V(Passive),Sheet Entry LD--V(Passive),Sheet Entry LD--V(Passive),Net Label GND,Net Label GND,Net Label GND,Net Label GND,Net Label GND,Power Object GND,Power Object GND)
Warning	LED Amplifier Dual.SchDoc	NetU2_3 contains Input Pin and Unspecified Port objects (Port IN A)
Warning	LED Amplifier Dual.SchDoc	NetU2_5 contains Input Pin and Unspecified Port objects (Port IN B)
Warning	LED Amplifier Dual.SchDoc	NetU3_3 contains Input Pin and Unspecified Port objects (Port IN A)
Warning	LED Amplifier Dual.SchDoc	NetU3_5 contains Input Pin and Unspecified Port objects (Port IN B)
Warning	LED Amplifier Single.SchDoc	NetU5_3 contains Input Pin and Unspecified Port objects (Port IN A)
Warning	LED Amplifier Dual.SchDoc	NetU6_3 contains Input Pin and Unspecified Port objects (Port IN A)
Warning	LED Amplifier Dual.SchDoc	NetU6_5 contains Input Pin and Unspecified Port objects (Port IN B)
Warning	LED Amplifier Dual.SchDoc	NetU7_3 contains Input Pin and Unspecified Port objects (Port IN A)
Warning	LED Amplifier Dual.SchDoc	NetU7_5 contains Input Pin and Unspecified Port objects (Port IN B)

Quantity	Value	Description	Designator	Footprint	LibRef
2	DNP	Capacitor	C1, C2	1206 Cap Small	Cap
6	0.1uF	Capacitor	C3, C4, C5, C6, C7, C8	1206 Cap Small	Cap Surface Mount, Cap
10	LTST-C150GKT	LED 1206	D1, D2, D3, D4, D5, D6, D7, D8, D9, PWR1	1206 LED	LED 1206
1	LTST-C150CKT	LED 1206	FAULT1	1206 LED	LED 1206
1	2 Port Plug	2 Port Terminal Plug	HDR1		Terminal Plug (2 Port) Mechanical
2	DSUB 37P VRT F PCB		J1, J2	DSUB1.385-2H37A Female - duplicate	PXle 2727, NI 9205
1	2 Pin Header	2 Pin Terminal Header	P1	Terminal Header(2 PIN)	Terminal Header (2 PIN)
1	PTC 30V 5A		PTC1	PTC 0ZRM0110FF1E	PTC
9	3.92K	Resistor	R1, R2, R3, R4, R5, R6, R7, R8, R9	1206 Passive	Resistor
2	1.5K 1W	Resistor	R10, R11	Resistor 2512	Resistor
9	510R	Resistor	R12, R13, R14, R15, R16, R17, R18, R19, R20	1206 Passive	Resistor
10	Test Point Jack	Through Hole Test Point, Snap-In 052 Hole	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP GND1	Ground Test Point	Test Point Jack TH
1	18-28V IN 9V 3W OUT ISO	Input 24volts regulates output to 5volts	U1	RS3-2405S Regulator	V REG 24V IN TO 5V OUT 1A
5	LT1490	Dual Channel, Micropower Operational Amplifier, 25mA output,, 2.4 to 40 V, 8-Pin SOIC (S8-8), Commercial	U2, U3, U5, U6, U7	LT-S8-8_N	LT1490
1	18-28V IN 5V 500MA OUT	Input 24volts regulates output to 5volts	U4	RECOM SIP-3 Regulator	V REG 24V IN TO 5V OUT 3 TERM