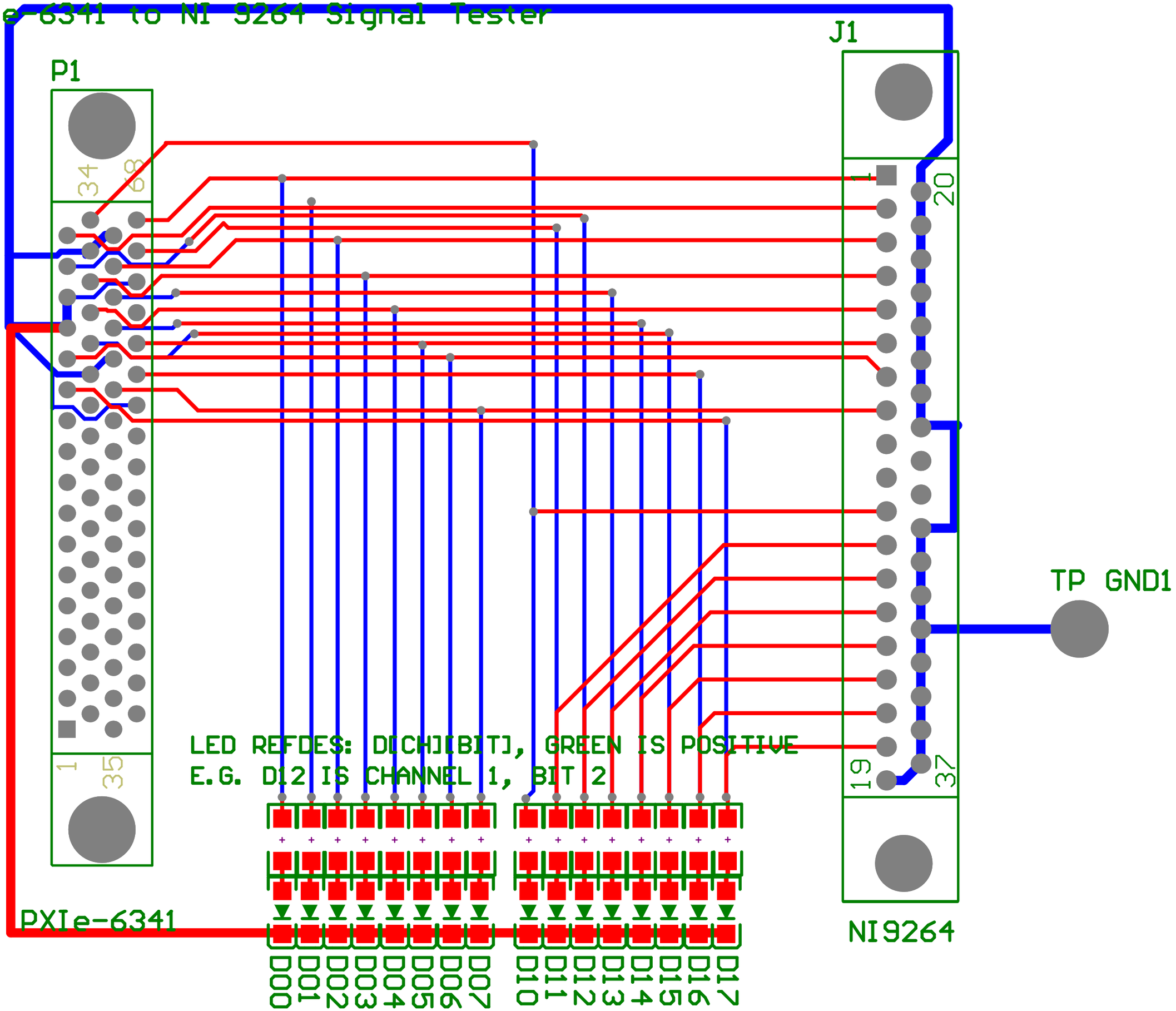
NSWCPD LBES NS18248 REV. A
PXIe-6341 to NI 9264 Signal Tester



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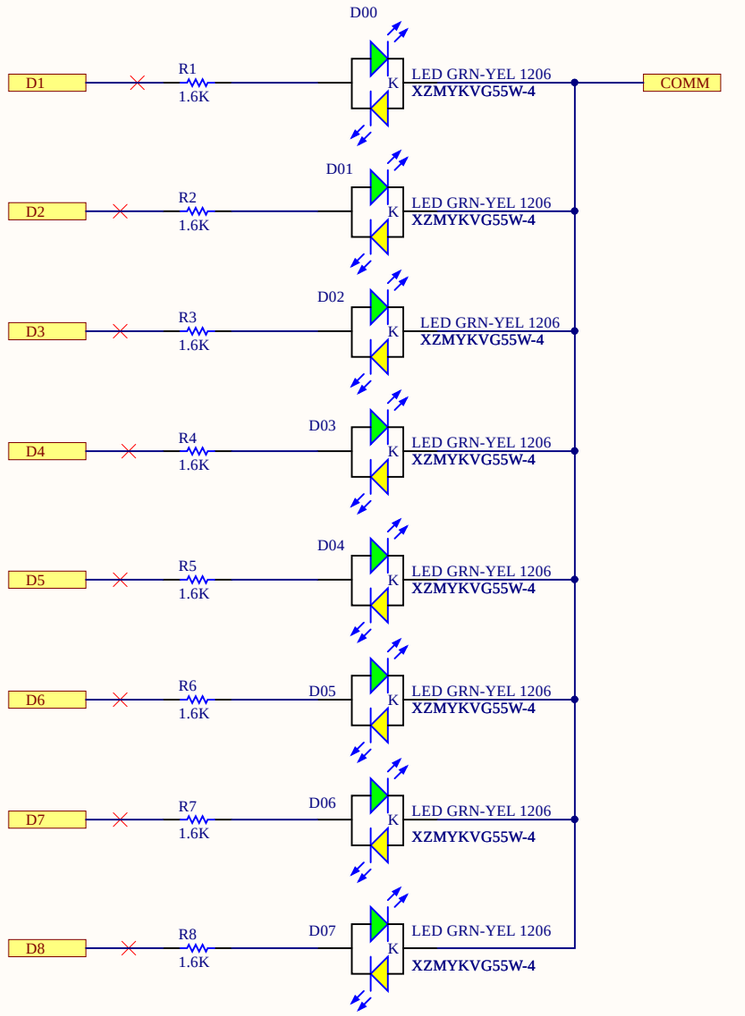
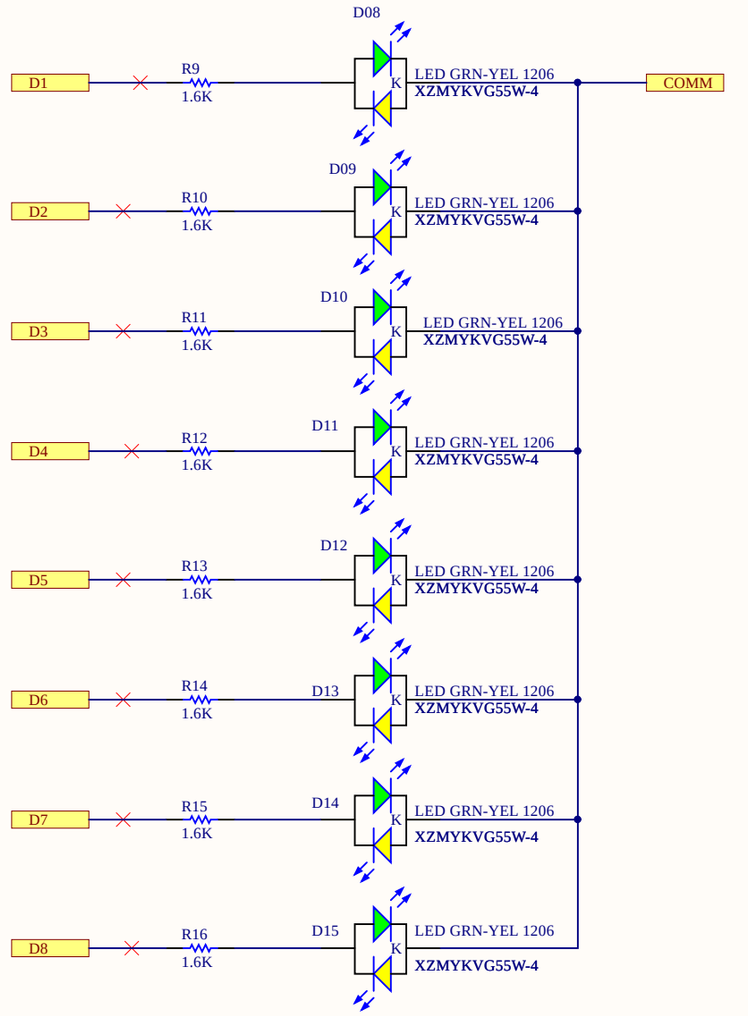


Title	***OCTAL LED ARRAY CC***		*NSWCPD* *901 Admiral Peary Way* *Building 77H Code 514* *Philadelphia, PA 19112*
Size: B	Number:NONE	Revision:A	
Date: 12/18/2018	Time: 10:01:16 AM	Sheet of	
File: C:\Users\Public\Documents\Altium\Projects\NS18248 PXIe 6341\LED Array Octal AC 5mA.SchDoc			

NAVSEA
NAVAL SEA SYSTEMS COMMAND
Land Based Engineering Site



Title	***OCTAL LED ARRAY CC***		*NSWCPD* *901 Admiral Peary Way* *Building 77H Code 514* *Philadelphia, PA 19112*
Size: B	Number:NONE	Revision:A	
Date: 12/18/2018	Time: 10:01:16 AM	Sheet of	
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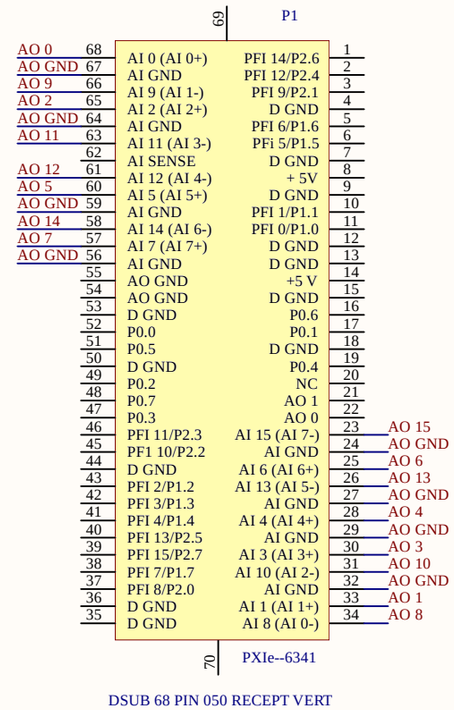
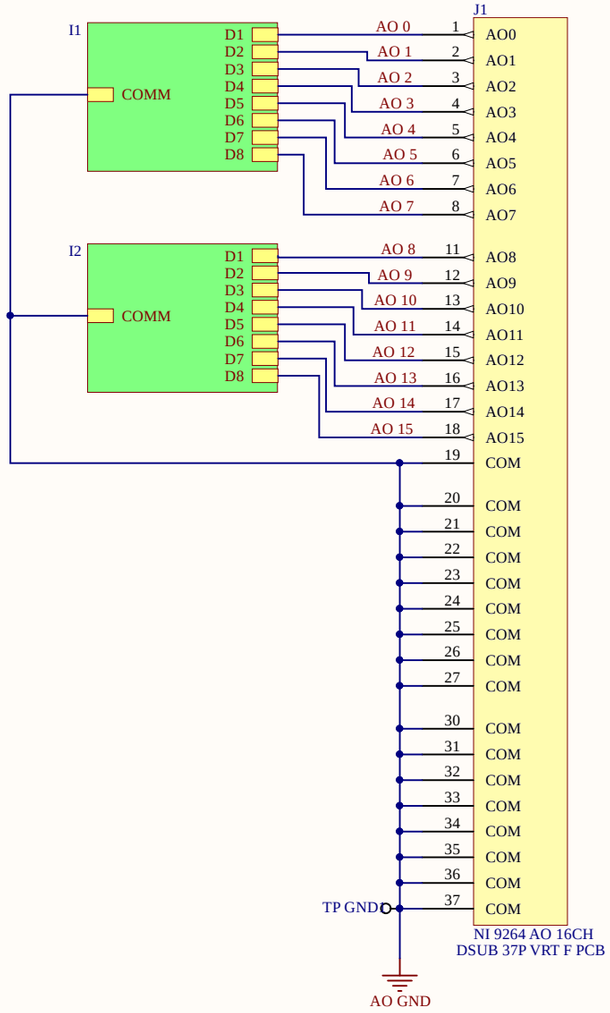
NAVSEA
NAVAL SEA SYSTEMS COMMAND
Land Based Engineering Site





Title	***PXIe 6341 to NI 9264***		*NSWCPD* *901 Admiral Peary Way* *Building 77H Code 514* *Philadelphia, PA 19112*
Size: B	Number: 18248RH01	Revision: A	
Date: 12/18/2018	Time: 10:01:16 AM	Sheet of	
File: C:\Users\Public\Documents\Altium\Projects\NS18248 PXIe 6341\NS18248 PXI 6341.SchDoc			

NAVSEA
NAVAL SEA SYSTEMS COMMAND
Land Based Engineering Site

NSWCPD LBES NS18248 REV. A
PXIe-6341 to NI 9264 Signal Tester

P1

PXIe-6341

J1

1

20

19

37

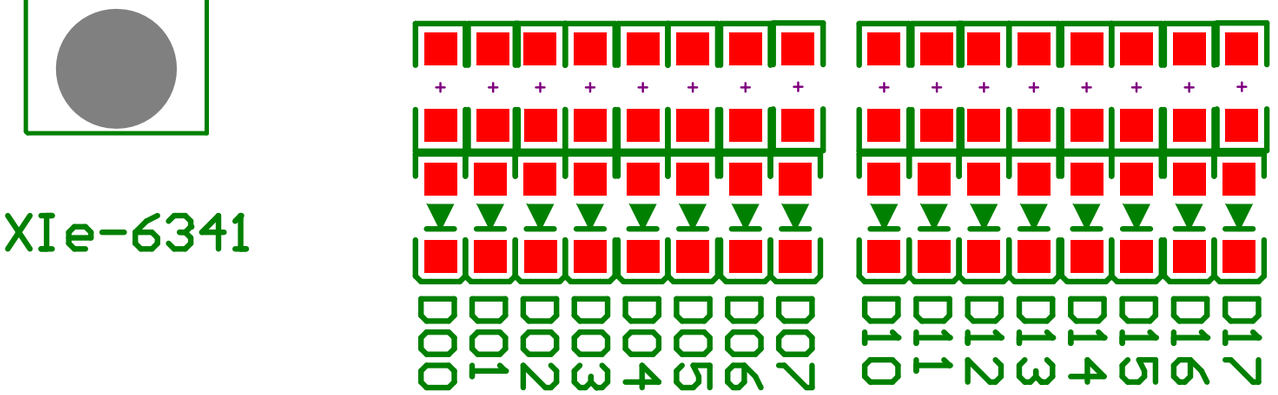
NI9264

TP GND1

LED REFDES: D[CH][BIT], GREEN IS POSITIVE
E.G. D12 IS CHANNEL 1, BIT 2

D00 D01 D02 D03 D04 D05 D06 D07

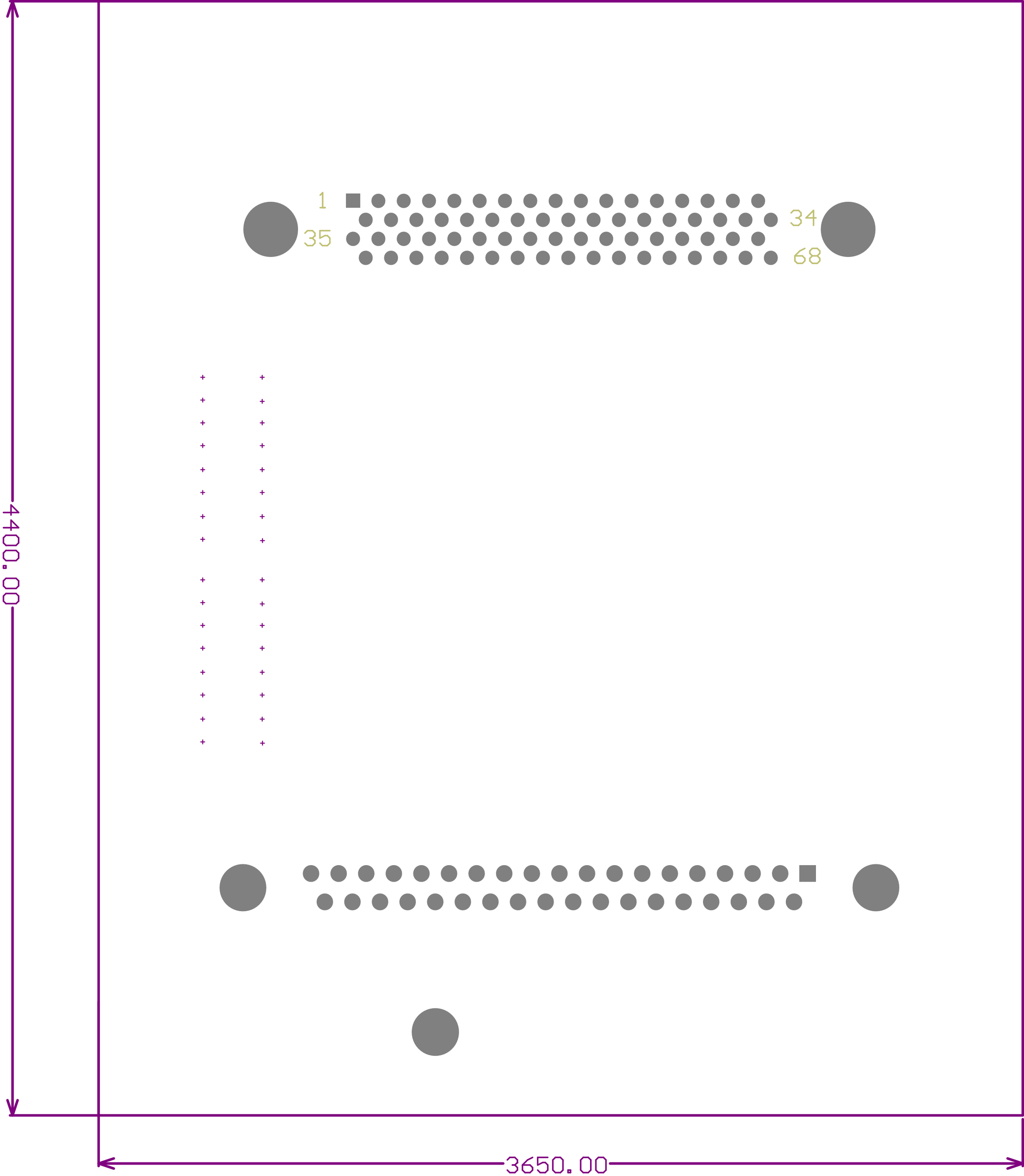
D10 D11 D12 D13 D14 D15 D16 D17



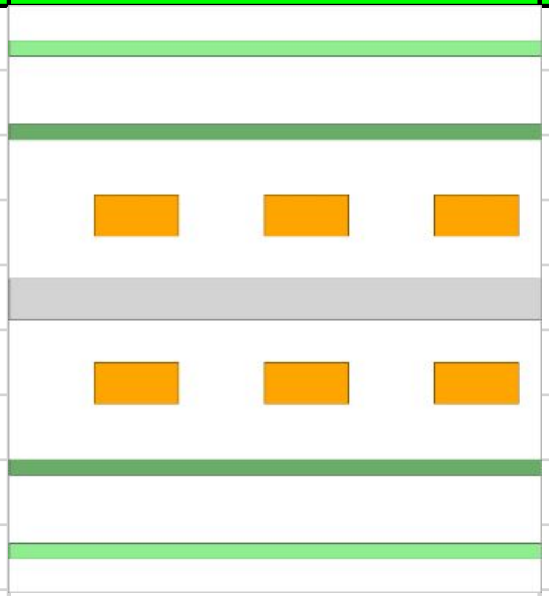
650.00

365

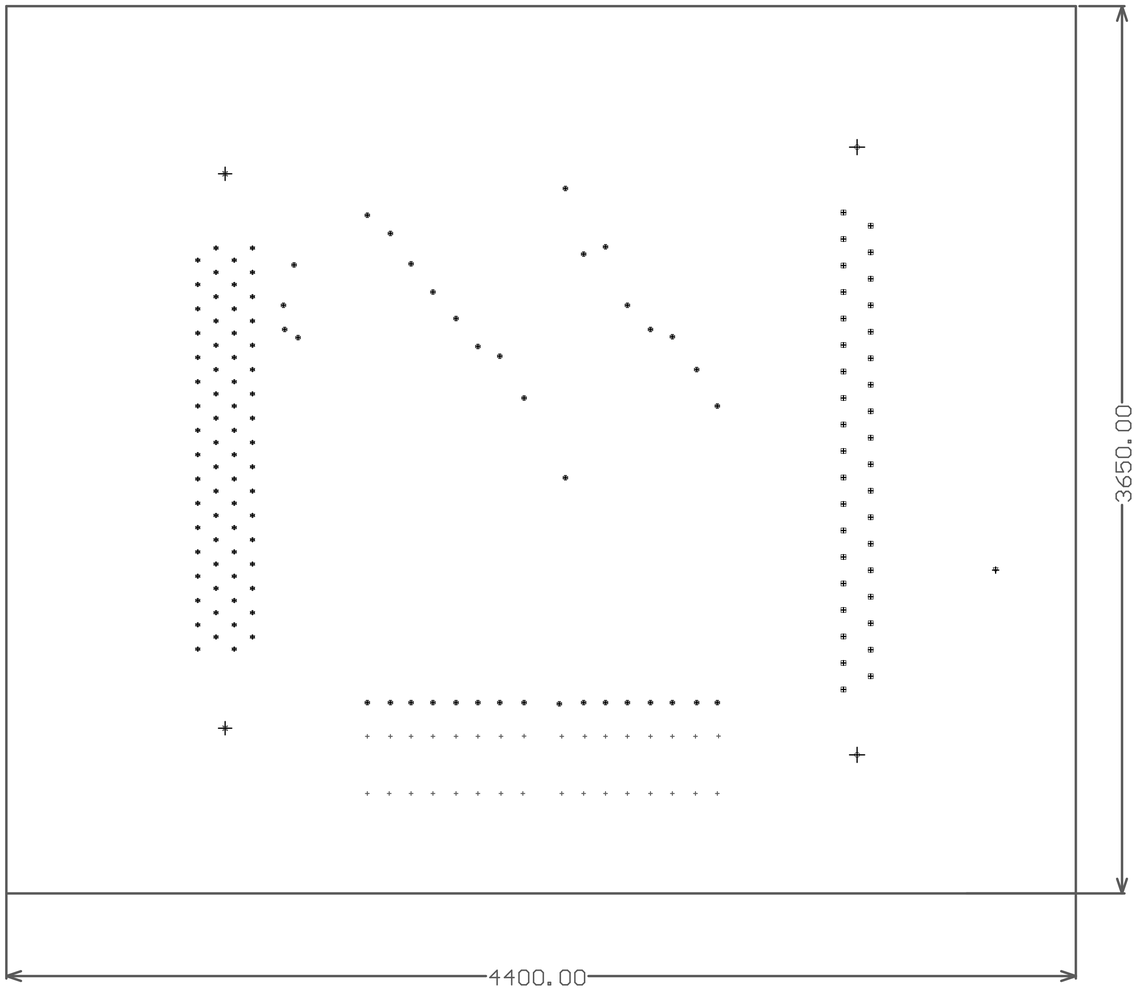
4400.00


1
35
34
68
4400.00
3650.00

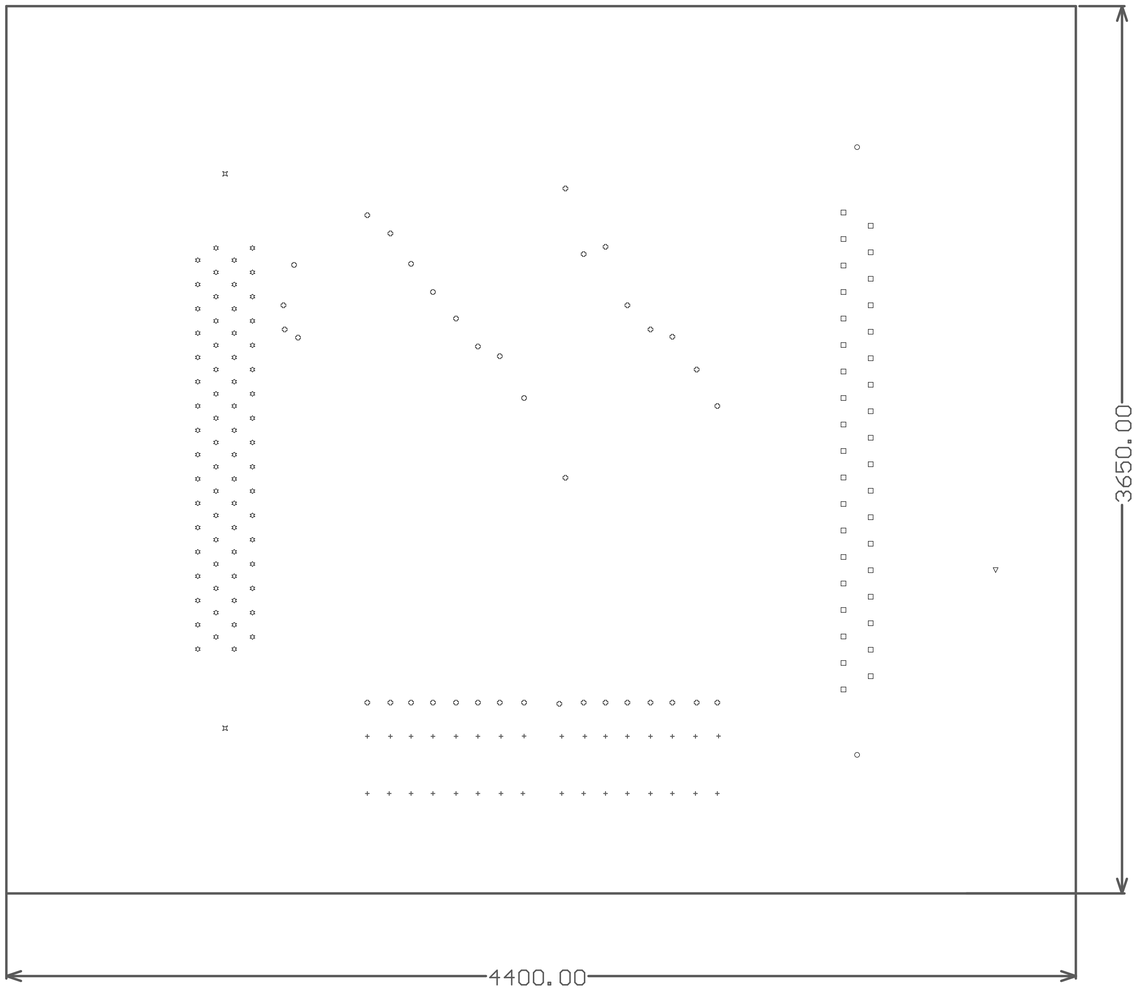
Board Stack Report

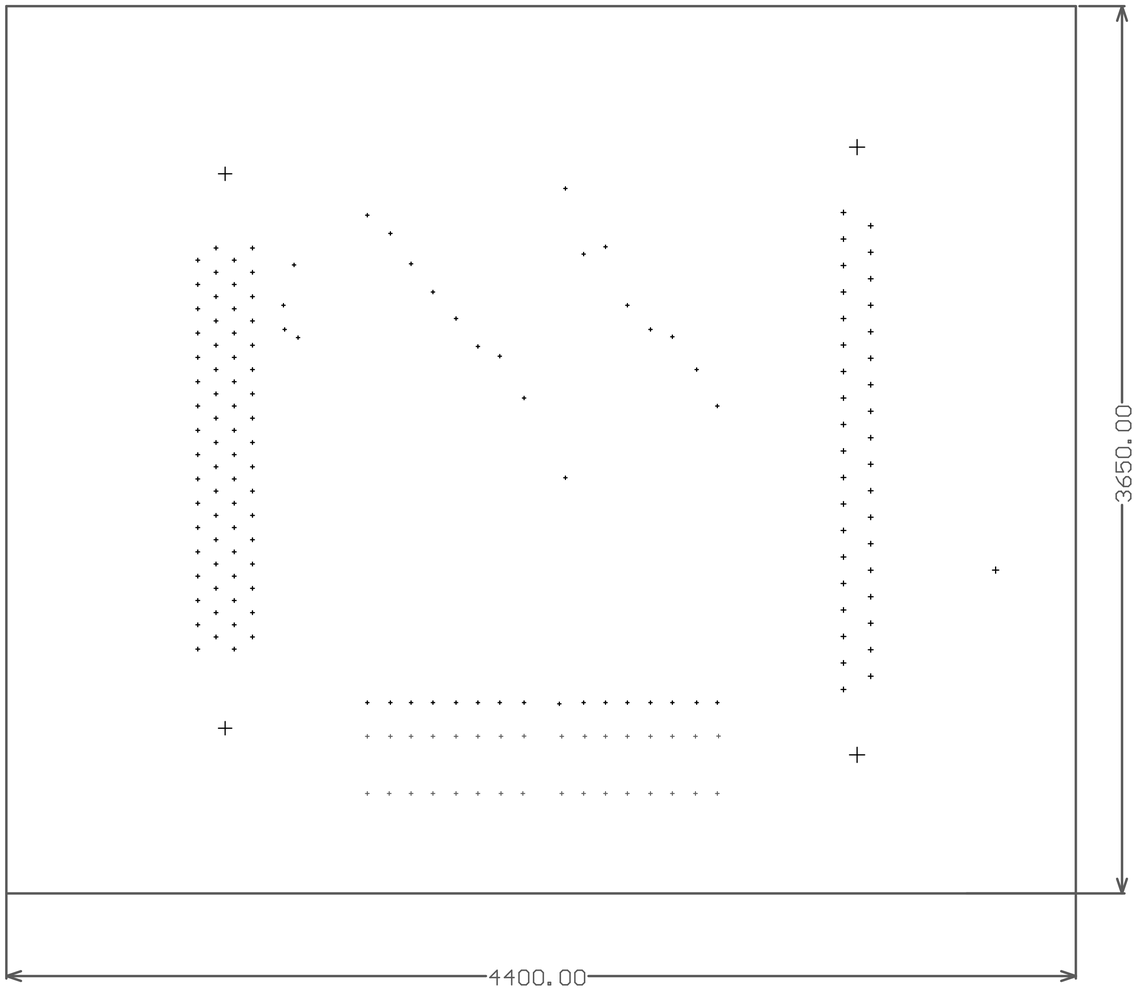
Stack Up		Layer Stack			
Layer	Board Layer Stack	Name	Material	Thickness	Constant
1		Top Paste			
2		Top Overlay			
3		Top Solder	Solder Resist	0.40mil	3.5
4		Top Layer	Copper	1.40mil	
5		Dielectric 1	FR-4	59.00mil	4.8
6		Bottom Layer	Copper	1.40mil	
7		Bottom Solder	Solder Resist	0.40mil	3.5
8		Bottom Overlay			
9		Bottom Paste			
	Height : 62.60mil				

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Template	Description	Hole Tolerance (+)	Hole Tolerance (-)
▽	1	52.00mil (1.321mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c475h132			
⛛	2	110.24mil (2.800mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c550h280			
○	2	125.00mil (3.175mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c470h318			
⛝	37	14.00mil (0.356mm)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	v71h36			
□	37	40.00mil (1.016mm)	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)			
✡	68	31.50mil (0.800mm)	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)			
	147 Total										



Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Template	Description	Hole Tolerance (+)	Hole Tolerance (-)
▽	1	52.00mil (1.321mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c475h132			
⌑	2	110.24mil (2.800mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c550h280			
○	2	125.00mil (3.175mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c470h318			
✣	37	14.00mil (0.356mm)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	v71h36			
□	37	40.00mil (1.016mm)	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)			
✡	68	31.50mil (0.800mm)	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)			
	147 Total										

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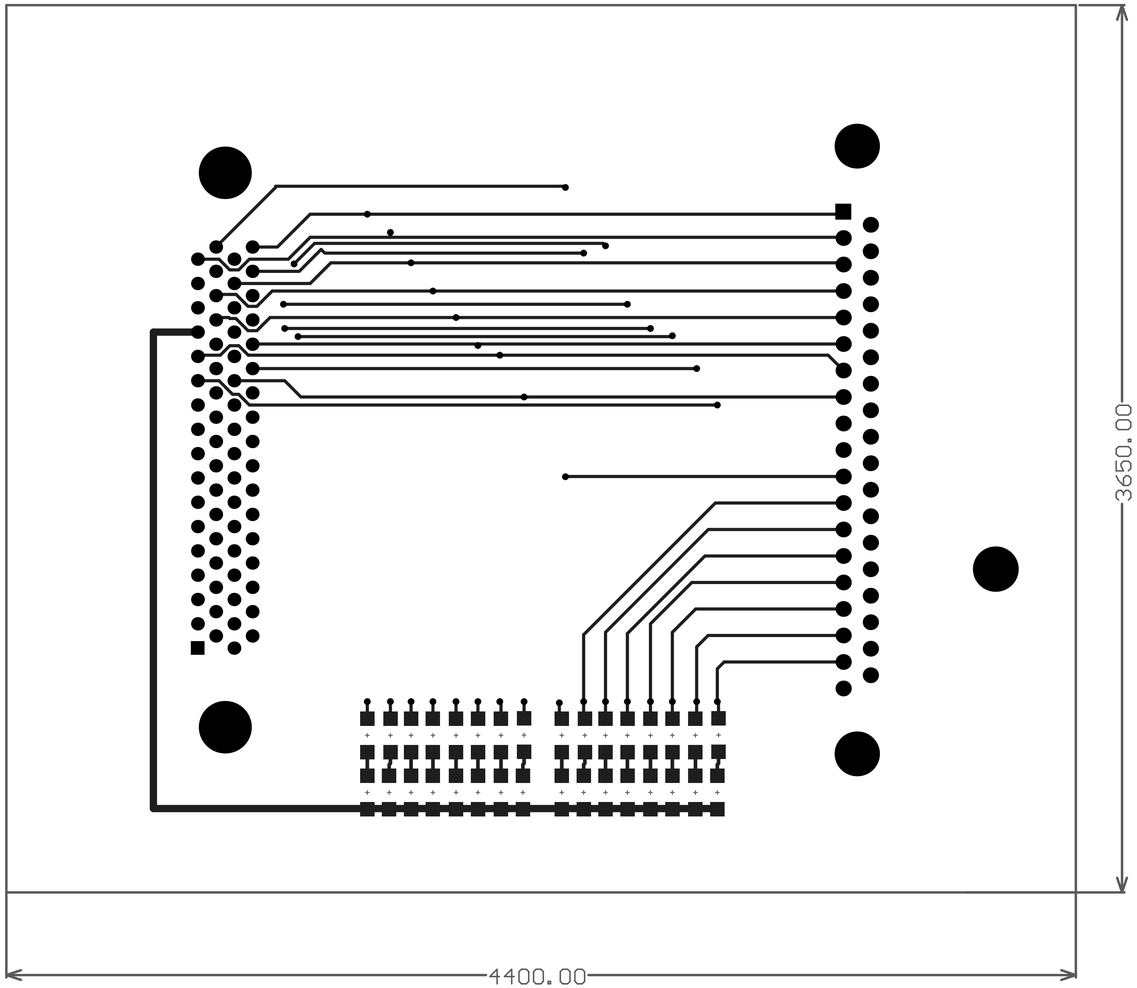
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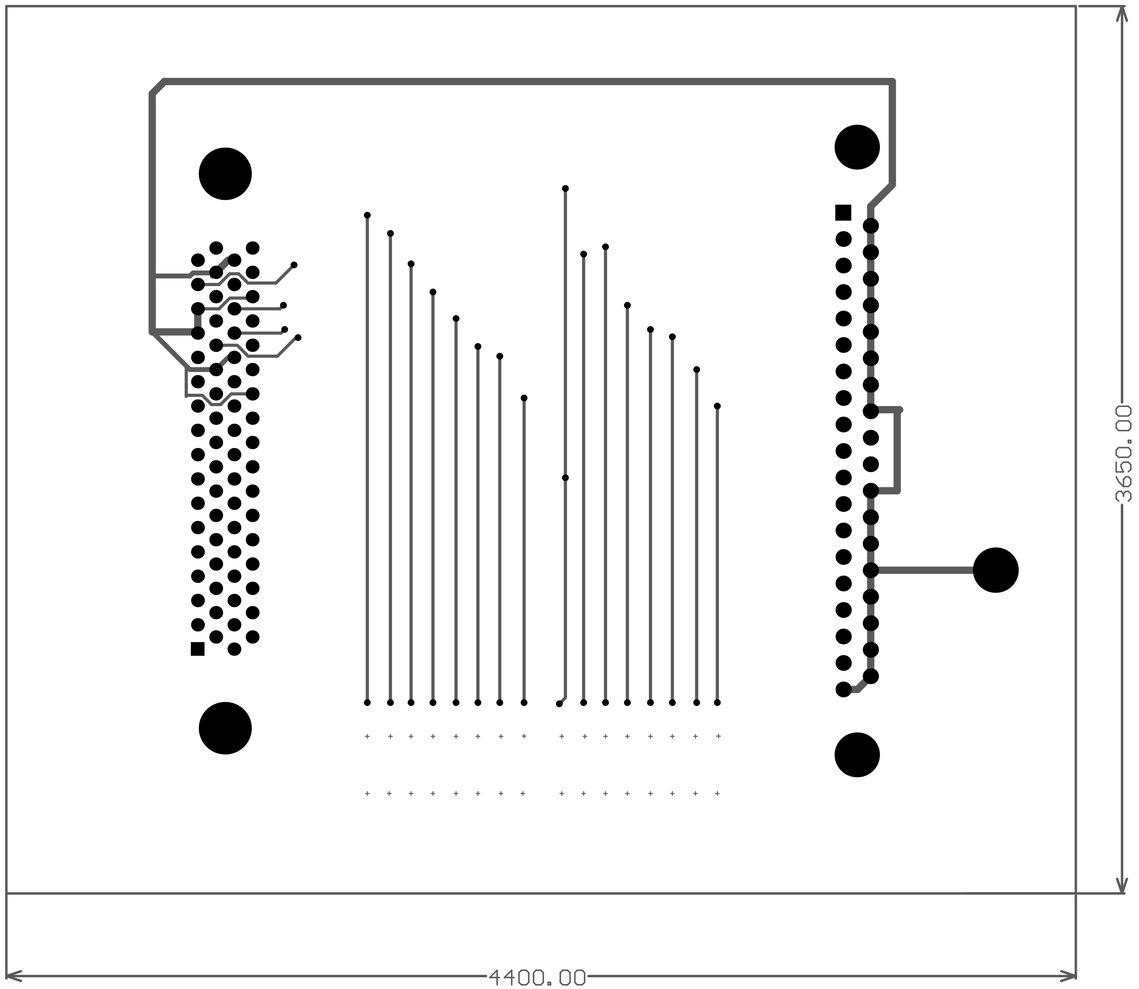
3650.00
4400.00


3650.00
4400.00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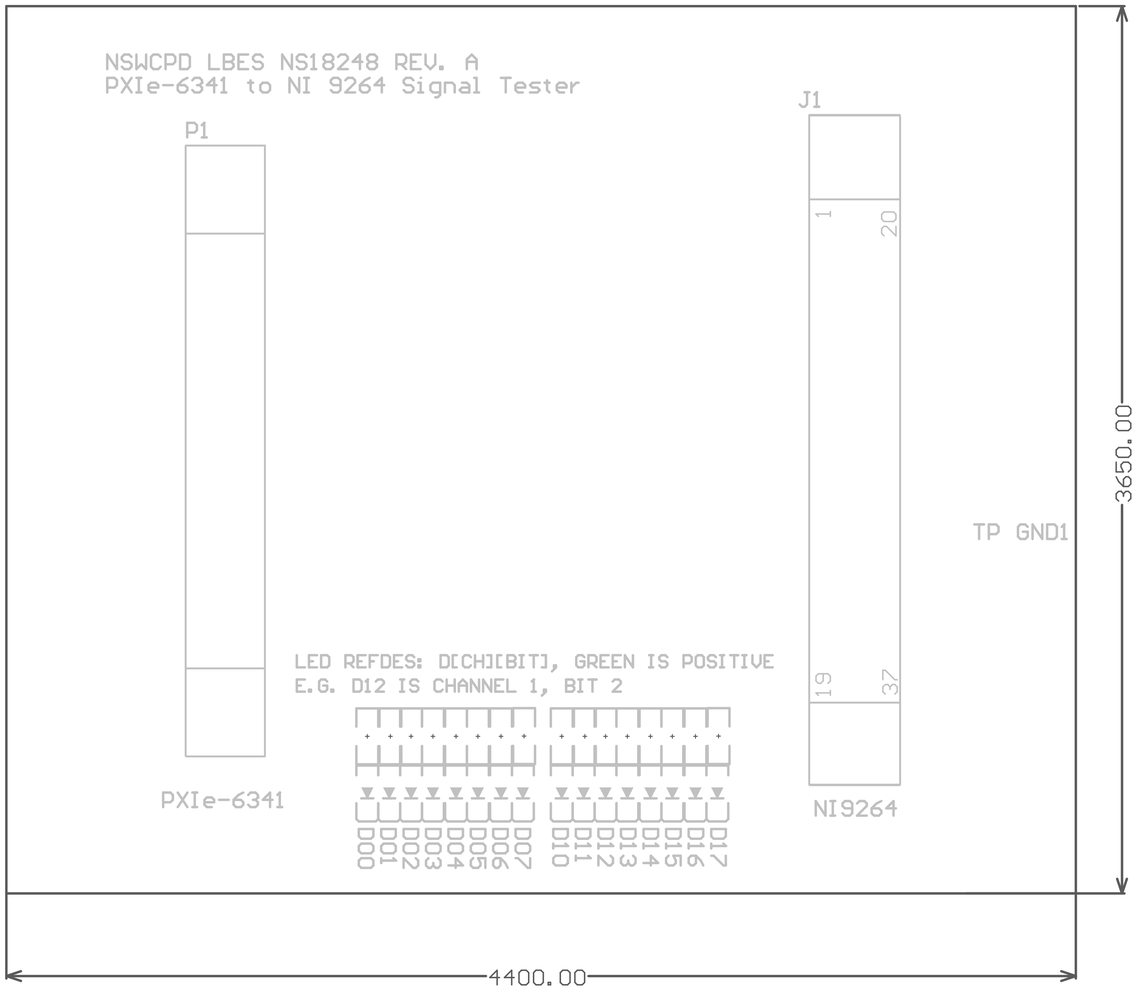
NSWCPD LBES NS18248 REV. A
PXIe-6341 to NI 9264 Signal Tester
P1
J1
1
20
19
37
TP GND1
LED REFDES: D[CH][BIT], GREEN IS POSITIVE
E.G. D12 IS CHANNEL 1, BIT 2
PXIe-6341
NI9264
D00
D01
D02
D03
D04
D05
D06
D07
D10
D11
D12
D13
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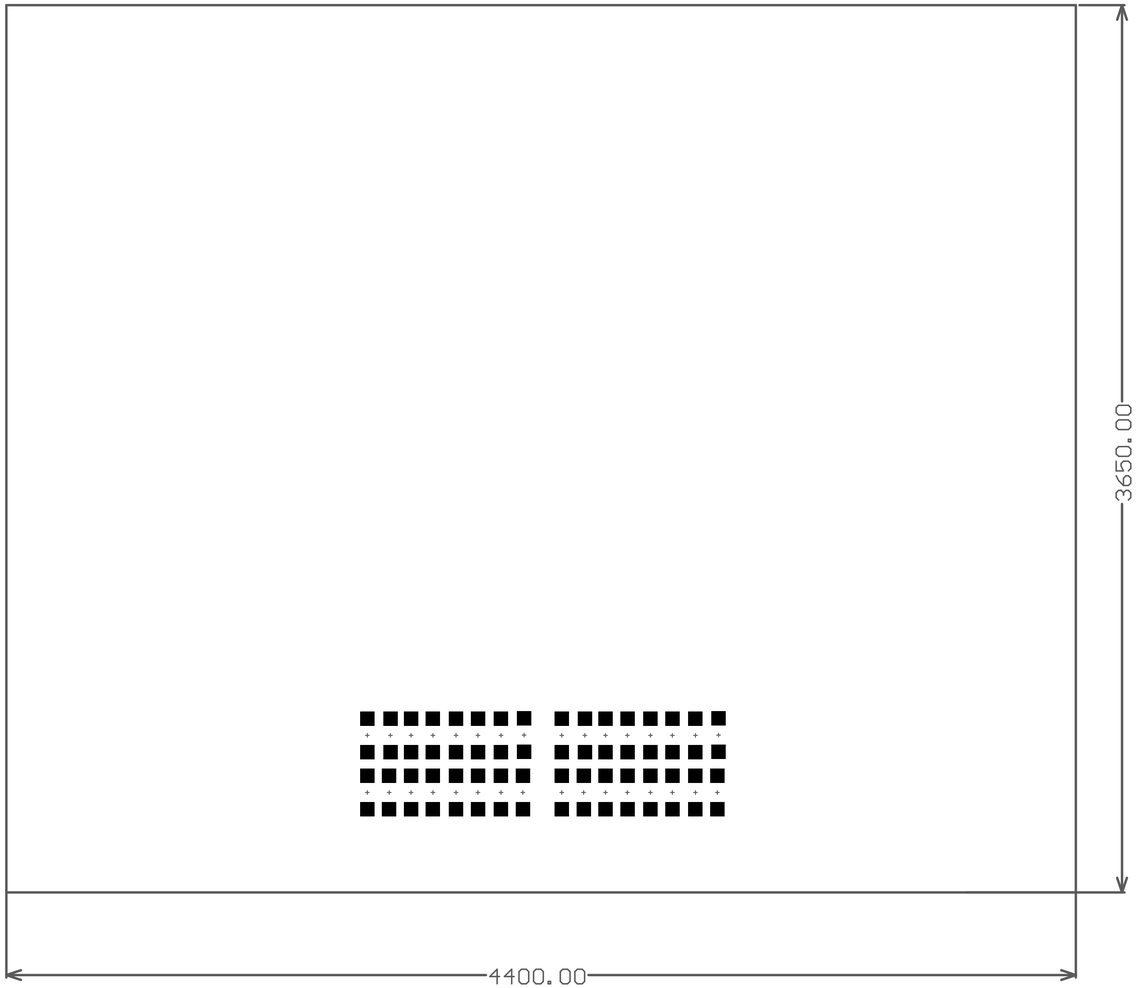
D15
D16
D17
3650.00
4400.00


34
68
1
35
3650.00
4400.00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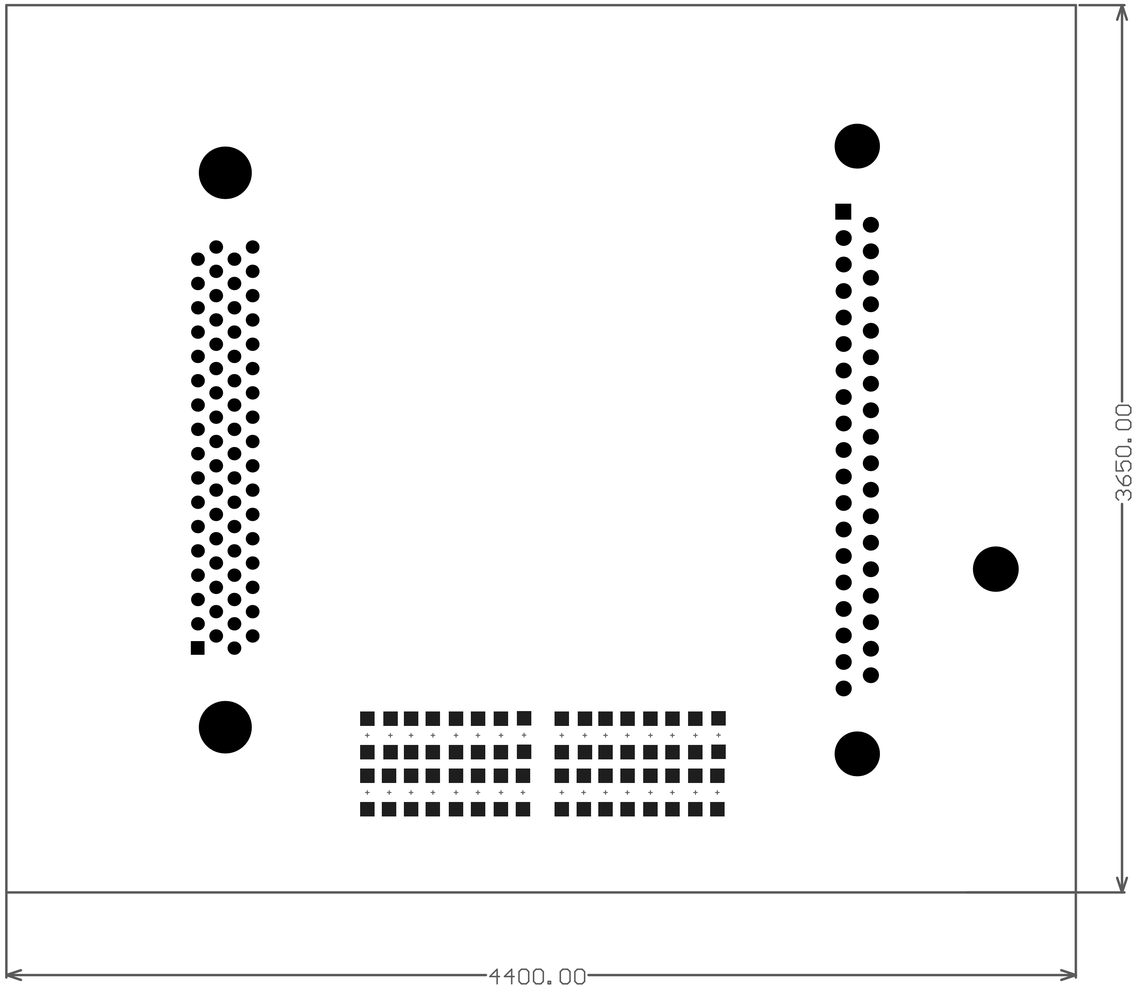
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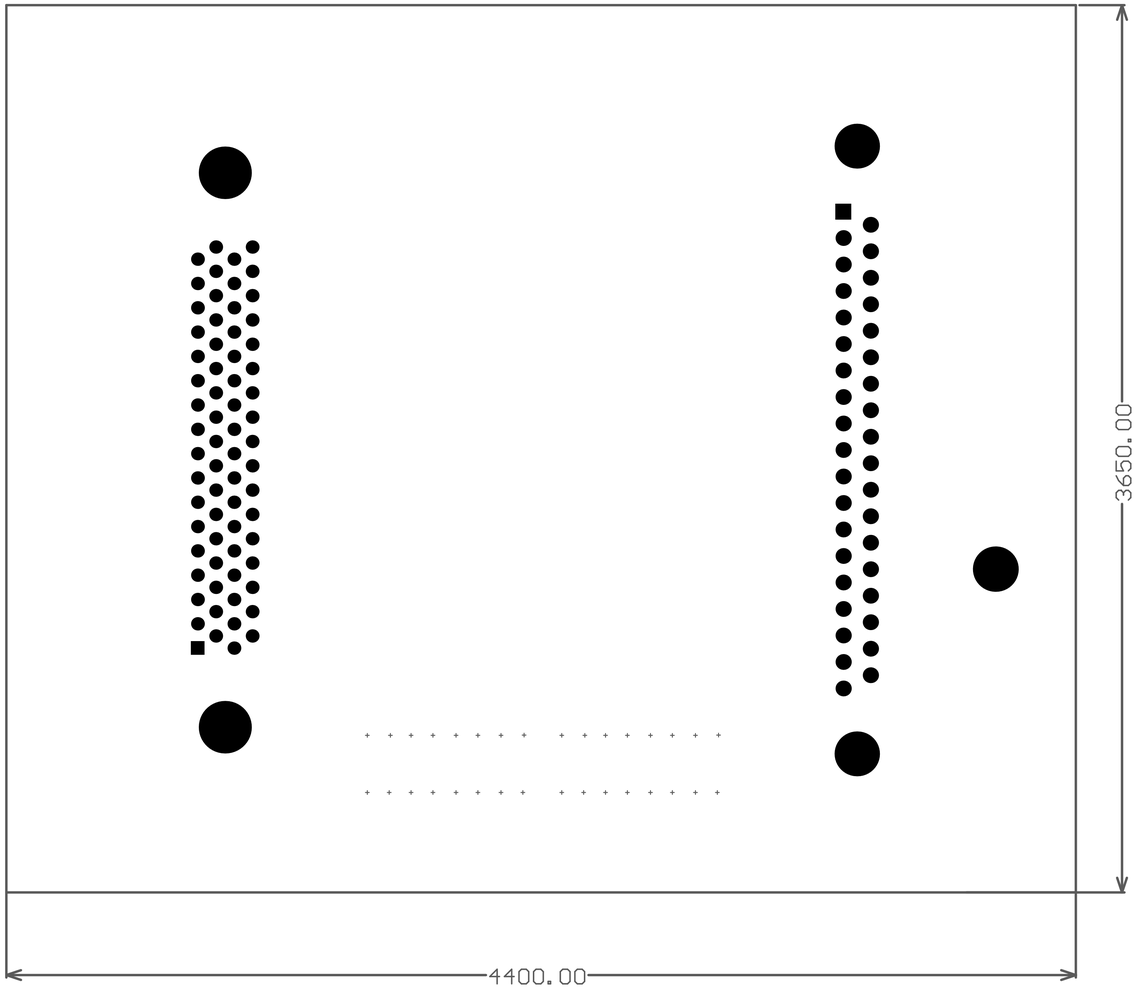
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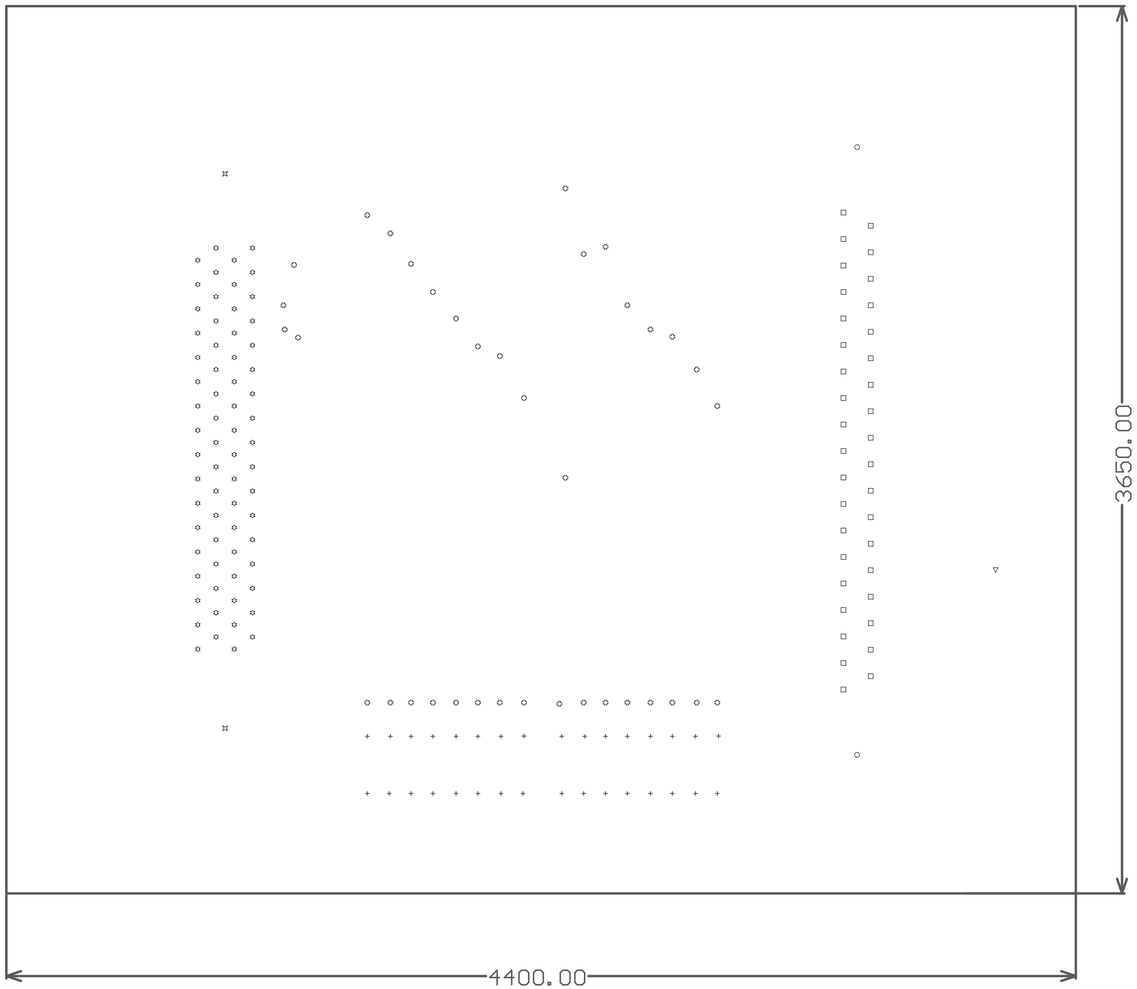
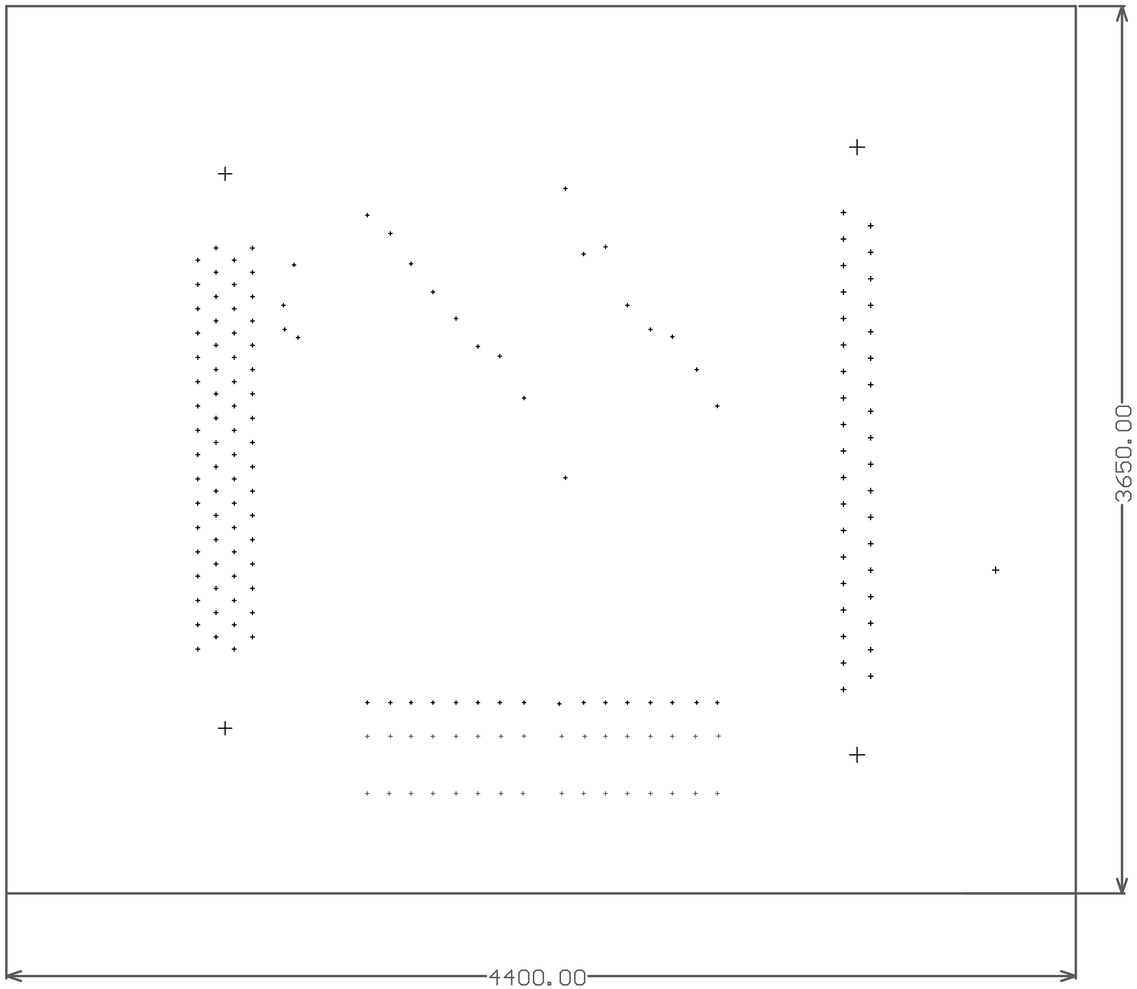
Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Template	Description	Hole Tolerance (+)	Hole Tolerance (-)
▽	1	52.00mil (1.321mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c475h132			
⌑	2	110.24mil (2.800mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c550h280			
○	2	125.00mil (3.175mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c470h318			
✣	37	14.00mil (0.356mm)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	v71h36			
□	37	40.00mil (1.016mm)	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)			
✡	68	31.50mil (0.800mm)	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)			
	147 Total										

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Design Rules Verification Report

Filename : C:\Users\Public\Documents\Altium\Projects\NS18248 PXIe 6341\Project Logs for NS18248 PXI 6341\NS18248 PXI 6341.PcbDoc

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=10mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=13mil) (Max=30mil) (Preferred=15mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Hole Size Constraint (Min=1mil) (Max=400mil) (All)	0
Pads and Vias to follow the Drill pairs settings	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Room I2 (Bounding Region = (3225mil, 1281.102mil, 3990mil, 1781.102mil) (InComponentClass('I2'))	0
Room NS18248 PXI 6341 (Bounding Region = (1685mil, 1430mil, 5180mil, 4220mil) (InComponentClass('NS18248 PXI	0
Room I1 (Bounding Region = (2425mil, 1281.102mil, 3190mil, 1781.102mil) (InComponentClass('I1'))	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Total	0

Electrical Rules Check Report

Class	Document	Message
Warning	NS18248 PXI 6341.SchDoc	AO 0 contains Output Pin and Unspecified Sheet Entry objects (Sheet Entry I1-D1(Passive))
Warning	NS18248 PXI 6341.SchDoc	AO 1 contains Output Pin and Unspecified Sheet Entry objects (Sheet Entry I1-D2(Passive))
Warning	NS18248 PXI 6341.SchDoc	AO 2 contains Output Pin and Unspecified Sheet Entry objects (Sheet Entry I1-D3(Passive))
Warning	NS18248 PXI 6341.SchDoc	AO 3 contains Output Pin and Unspecified Sheet Entry objects (Sheet Entry I1-D4(Passive))
Warning	NS18248 PXI 6341.SchDoc	AO 4 contains Output Pin and Unspecified Sheet Entry objects (Sheet Entry I1-D5(Passive))
Warning	NS18248 PXI 6341.SchDoc	AO 5 contains Output Pin and Unspecified Sheet Entry objects (Sheet Entry I1-D6(Passive))
Warning	NS18248 PXI 6341.SchDoc	AO 6 contains Output Pin and Unspecified Sheet Entry objects (Sheet Entry I1-D7(Passive))
Warning	NS18248 PXI 6341.SchDoc	AO 7 contains Output Pin and Unspecified Sheet Entry objects (Sheet Entry I1-D8(Passive))
Warning	NS18248 PXI 6341.SchDoc	AO 8 contains Output Pin and Unspecified Sheet Entry objects (Sheet Entry I2-D1(Passive))
Warning	NS18248 PXI 6341.SchDoc	AO 9 contains Output Pin and Unspecified Sheet Entry objects (Sheet Entry I2-D2(Passive))
Warning	NS18248 PXI 6341.SchDoc	AO 10 contains Output Pin and Unspecified Sheet Entry objects (Sheet Entry I2-D3(Passive))
Warning	NS18248 PXI 6341.SchDoc	AO 11 contains Output Pin and Unspecified Sheet Entry objects (Sheet Entry I2-D4(Passive))
Warning	NS18248 PXI 6341.SchDoc	AO 12 contains Output Pin and Unspecified Sheet Entry objects (Sheet Entry I2-D5(Passive))
Warning	NS18248 PXI 6341.SchDoc	AO 13 contains Output Pin and Unspecified Sheet Entry objects (Sheet Entry I2-D6(Passive))
Warning	NS18248 PXI 6341.SchDoc	AO 14 contains Output Pin and Unspecified Sheet Entry objects (Sheet Entry I2-D7(Passive))
Warning	NS18248 PXI 6341.SchDoc	AO 15 contains Output Pin and Unspecified Sheet Entry objects (Sheet Entry I2-D8(Passive))
Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO 0 has multiple names (Net Label AO 0,Net Label AO 0,Sheet Entry I1-D1(Passive))
Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO 0 has multiple names (Sheet Entry I1-D1(Passive),Net Label AO 0,Net Label AO 0)
Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO 1 has multiple names (Net Label AO 1,Net Label AO 1,Sheet Entry I1-D2(Passive))
Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO 1 has multiple names (Sheet Entry I1-D2(Passive),Net Label AO 1,Net Label AO 1)
Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO 2 has multiple names (Net Label AO 2,Net Label AO 2,Sheet Entry I1-D3(Passive))
Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO 2 has multiple names (Sheet Entry I1-D3(Passive),Net Label AO 2,Net Label AO 2)
Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO 3 has multiple names (Net Label AO 3,Net Label AO 3,Sheet Entry I1-D4(Passive))
Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO 3 has multiple names (Sheet Entry I1-D4(Passive),Net Label AO 3,Net Label AO 3)
Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO 4 has multiple names (Net Label AO 4,Net Label AO 4,Sheet Entry I1-D5(Passive))
Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO 4 has multiple names (Sheet Entry I1-D5(Passive),Net Label AO 4,Net Label AO 4)
Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO 5 has multiple names (Net Label AO 5,Net Label AO 5,Sheet Entry I1-D6(Passive))
Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO 5 has multiple names (Sheet Entry I1-D6(Passive),Net Label AO 5,Net Label AO 5)
Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO 6 has multiple names (Net Label AO 6,Net Label AO 6,Sheet Entry I1-D7(Passive))
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Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO 7 has multiple names (Net Label AO 7,Net Label AO 7,Sheet Entry I1-D8(Passive))
Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO 7 has multiple names (Sheet Entry I1-D8(Passive),Net Label AO 7,Net Label AO 7)
Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO 8 has multiple names (Net Label AO 8,Net Label AO 8,Sheet Entry I2-D1(Passive))
Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO 8 has multiple names (Sheet Entry I2-D1(Passive),Net Label AO 8,Net Label AO 8)
Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO 9 has multiple names (Net Label AO 9,Net Label AO 9,Sheet Entry I2-D2(Passive))
Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO 9 has multiple names (Sheet Entry I2-D2(Passive),Net Label AO 9,Net Label AO 9)
Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO 10 has multiple names (Net Label AO 10,Net Label AO 10,Sheet Entry I2-D3(Passive))
Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO 10 has multiple names (Sheet Entry I2-D3(Passive),Net Label AO 10,Net Label AO 10)
Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO 11 has multiple names (Net Label AO 11,Net Label AO 11,Sheet Entry I2-D4(Passive))

Class	Document	Message
Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO 11 has multiple names (Sheet Entry I2-D4(Passive),Net Label AO 11,Net Label AO 11)
Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO 12 has multiple names (Net Label AO 12,Net Label AO 12,Sheet Entry I2-D5(Passive))
Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO 12 has multiple names (Sheet Entry I2-D5(Passive),Net Label AO 12,Net Label AO 12)
Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO 13 has multiple names (Net Label AO 13,Net Label AO 13,Sheet Entry I2-D6(Passive))
Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO 13 has multiple names (Sheet Entry I2-D6(Passive),Net Label AO 13,Net Label AO 13)
Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO 14 has multiple names (Net Label AO 14,Net Label AO 14,Sheet Entry I2-D7(Passive))
Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO 14 has multiple names (Sheet Entry I2-D7(Passive),Net Label AO 14,Net Label AO 14)
Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO 15 has multiple names (Net Label AO 15,Net Label AO 15,Sheet Entry I2-D8(Passive))
Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO 15 has multiple names (Sheet Entry I2-D8(Passive),Net Label AO 15,Net Label AO 15)
Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO GND has multiple names (Net Label AO GND,Net Label AO GND,Net Label AO GND,Net Label AO GND,Net Label AO GND,Net Label AO GND,Net Label AO GND,Net Label AO GND,Power Object AO GND,Sheet Entry I1-COMM(Passive),Sheet Entry I2-COMM(Passive))
Warning	NS18248 PXI 6341.SchDoc	Nets Wire AO GND has multiple names (Sheet Entry I1-COMM(Passive),Sheet Entry I2-COMM(Passive),Net Label AO GND,Net Label AO GND,Net Label AO GND,Net Label AO GND,Net Label AO GND,Net Label AO GND,Net Label AO GND,Net Label AO GND,Power Object AO GND)

Quantity	Value	Description	Designator	Footprint	LibRef
16	LED GRN-YEL 1206	Back to back LEDs	D00, D01, D02, D03, D04, D05, D06, D07, D08, D09, D10, D11, D12, D13, D14, D15	1206 LED	LED GRN_YEL
1	DSUB 37P VRT F PCB		J1	DSUB1.385-2H37A FEMALE VRT	NI 9264 AO 16CH
1	DSUB 68 PIN 050 RECEPT VERT		P1	CHAMP1.27-2V68	PXIe-6341
16	1.6K	Resistor	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16	1206 Passive	Resistor
1	Test Point Jack	Through Hole Test Point, Snap-In 052 Hole	TP GND1	Ground Test Point	Test Point Jack TH