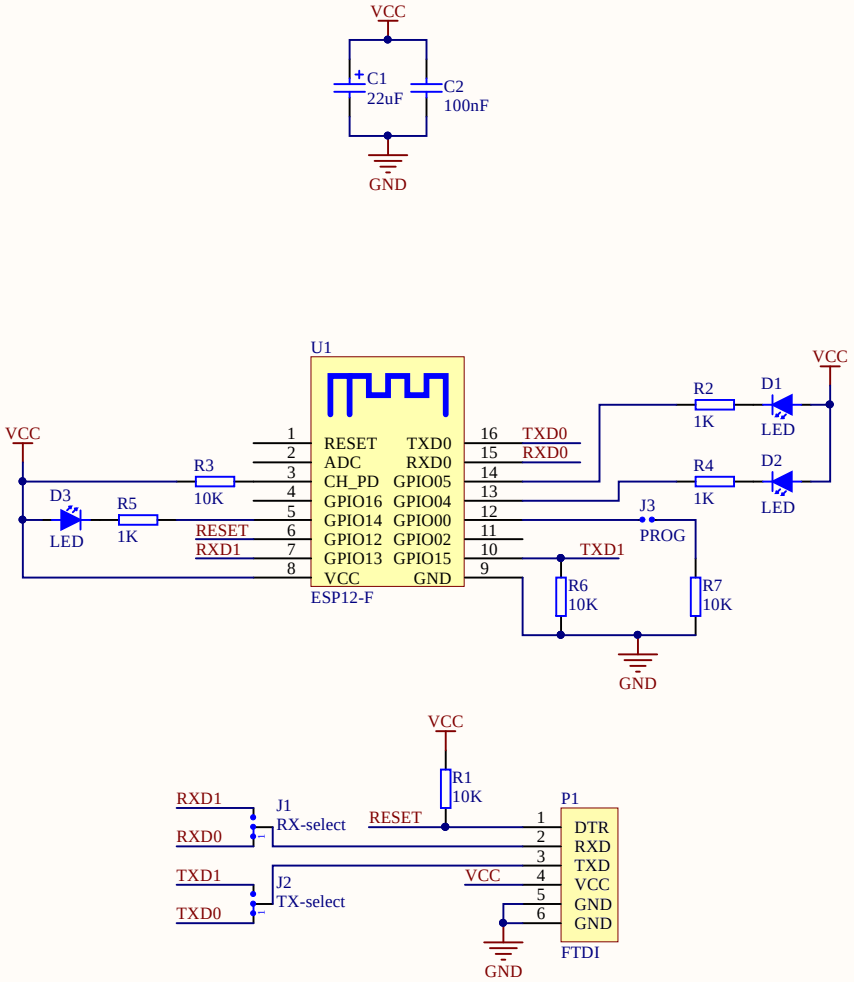


ESP2FTD V1.0 20160228

Bill of Materials

<Parameter Title not found>

Source Data From: esp2ftdi.PrjPcb

Project: esp2ftdi.PrjPcb

Variant: None

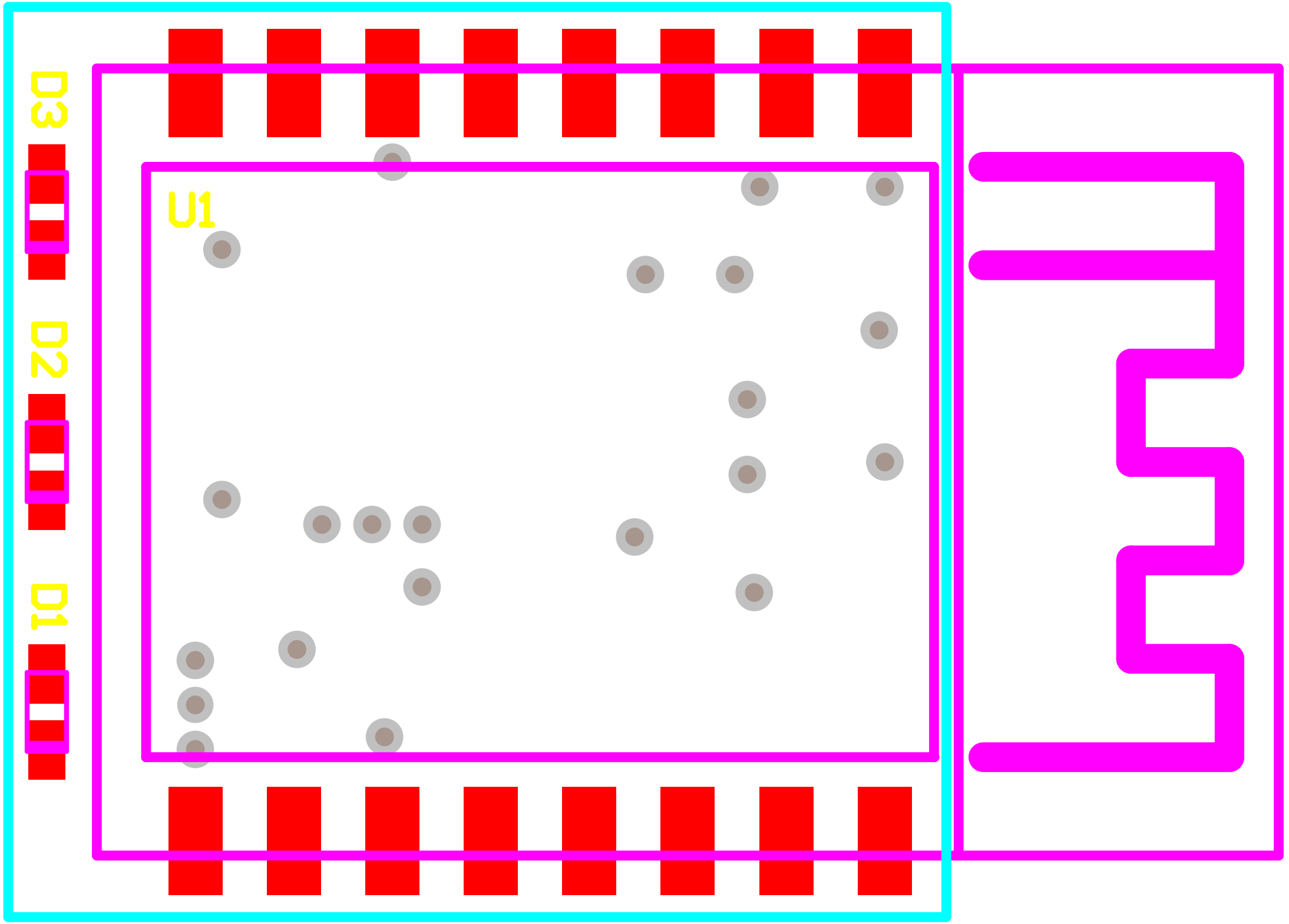
Creation Date: 28/02/2016 15:18:11

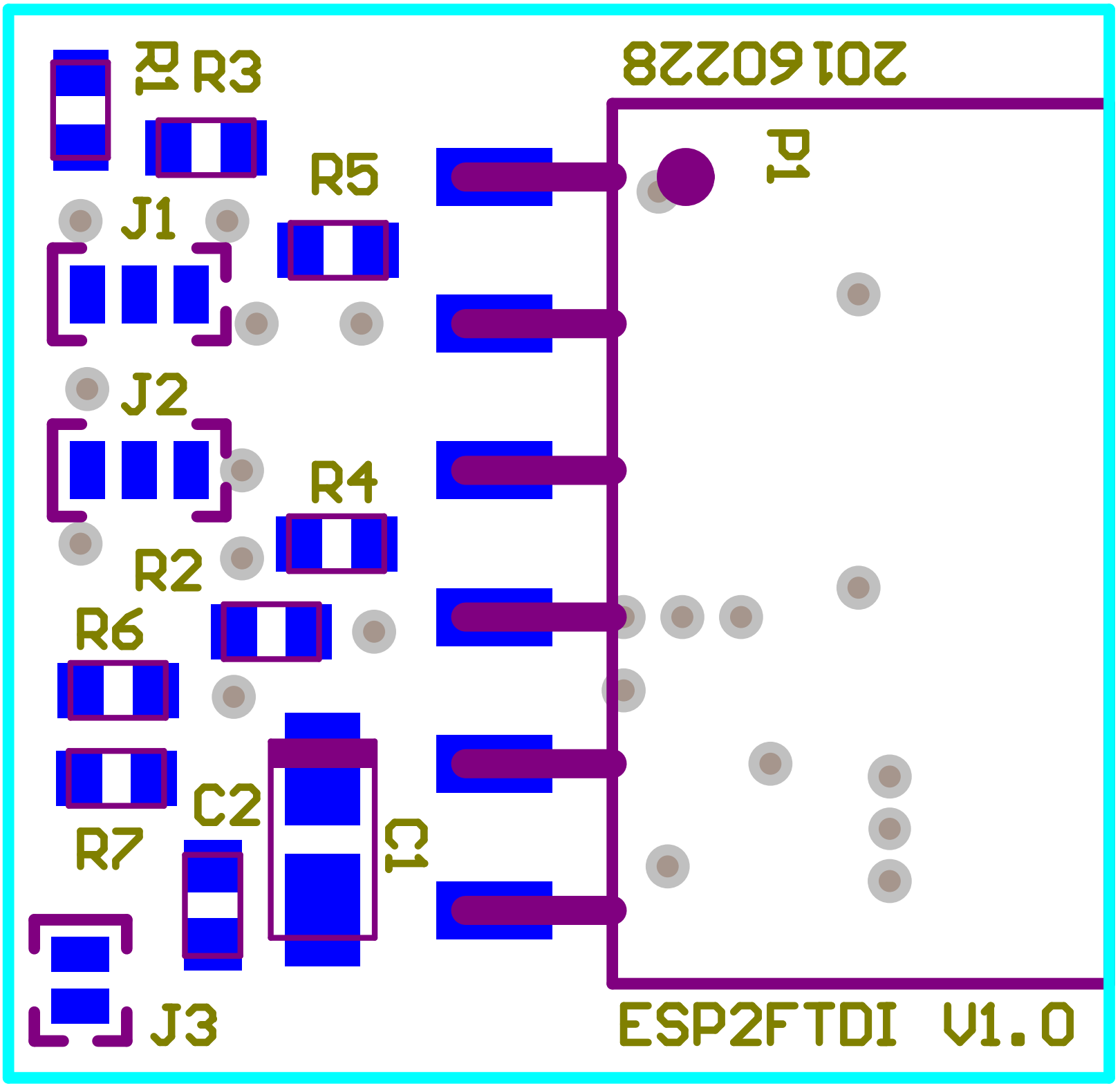
Print Date: 28-Feb-16 3:18:15 PM

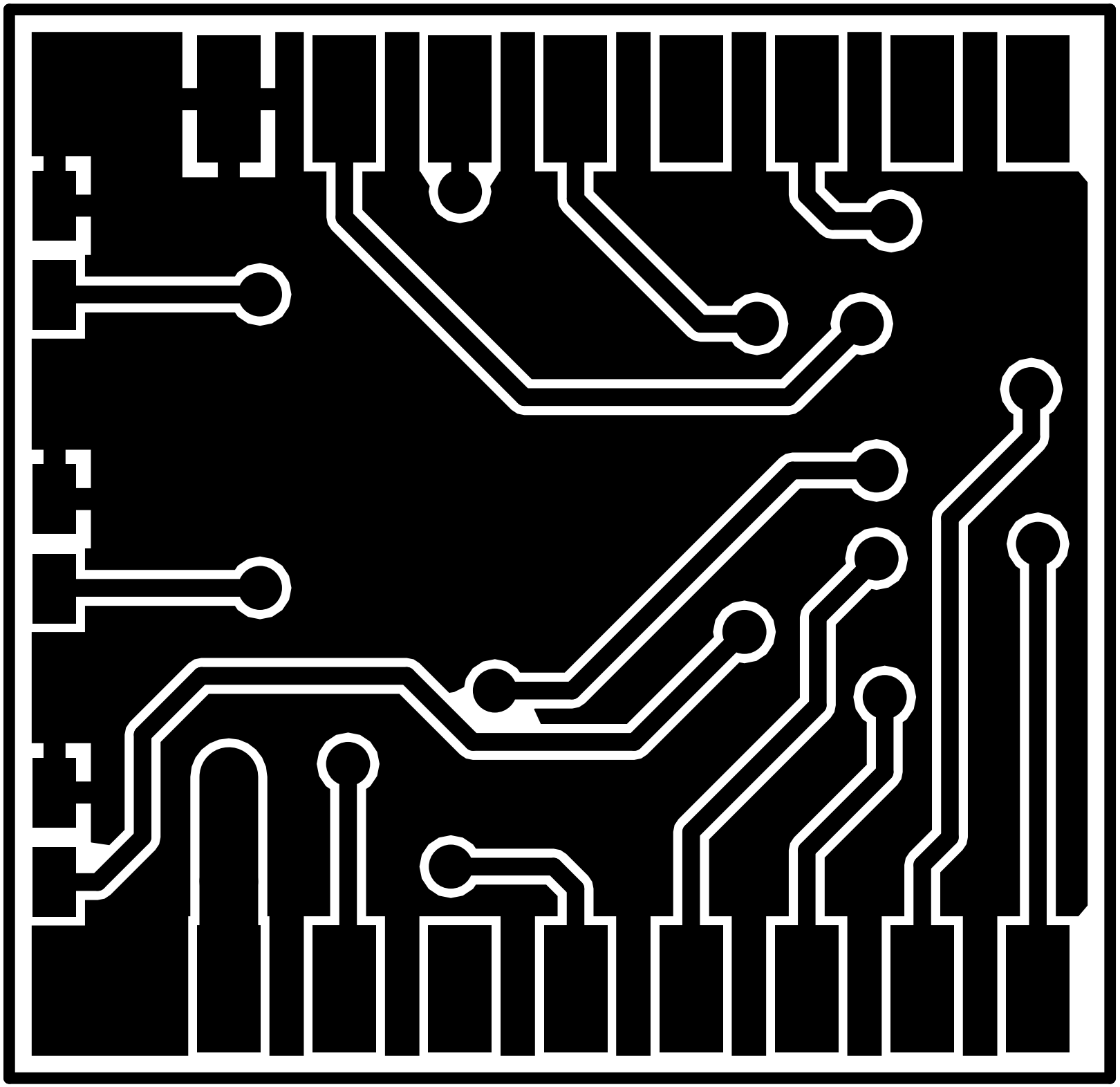
Footprint	Comment	LibRef	Designator	Description	Quantity
RESC1608X05N	10K	Resistor	R1, R3, R6, R7	Resistor	4
DIOM1608X04N	LED	LED	D1, D2, D3		3
RESC1608X05N	1K	Resistor	R2, R4, R5	Resistor	3
CAPMP3216X18N	22uF	Capacitor Polarized	C1	Capacitor Polarized	1
CAPC1608X05N	100nF	Capacitor	C2	Capacitor	1
ESP12-F	ESP12-F	ESP12-F	U1	ESP8266 based wireless module	1
HDR-SMD-1X6 -P2.54-female	FTDI	FTDI	P1	Basic FTDI Connector (Arduino compatible)	1
					14

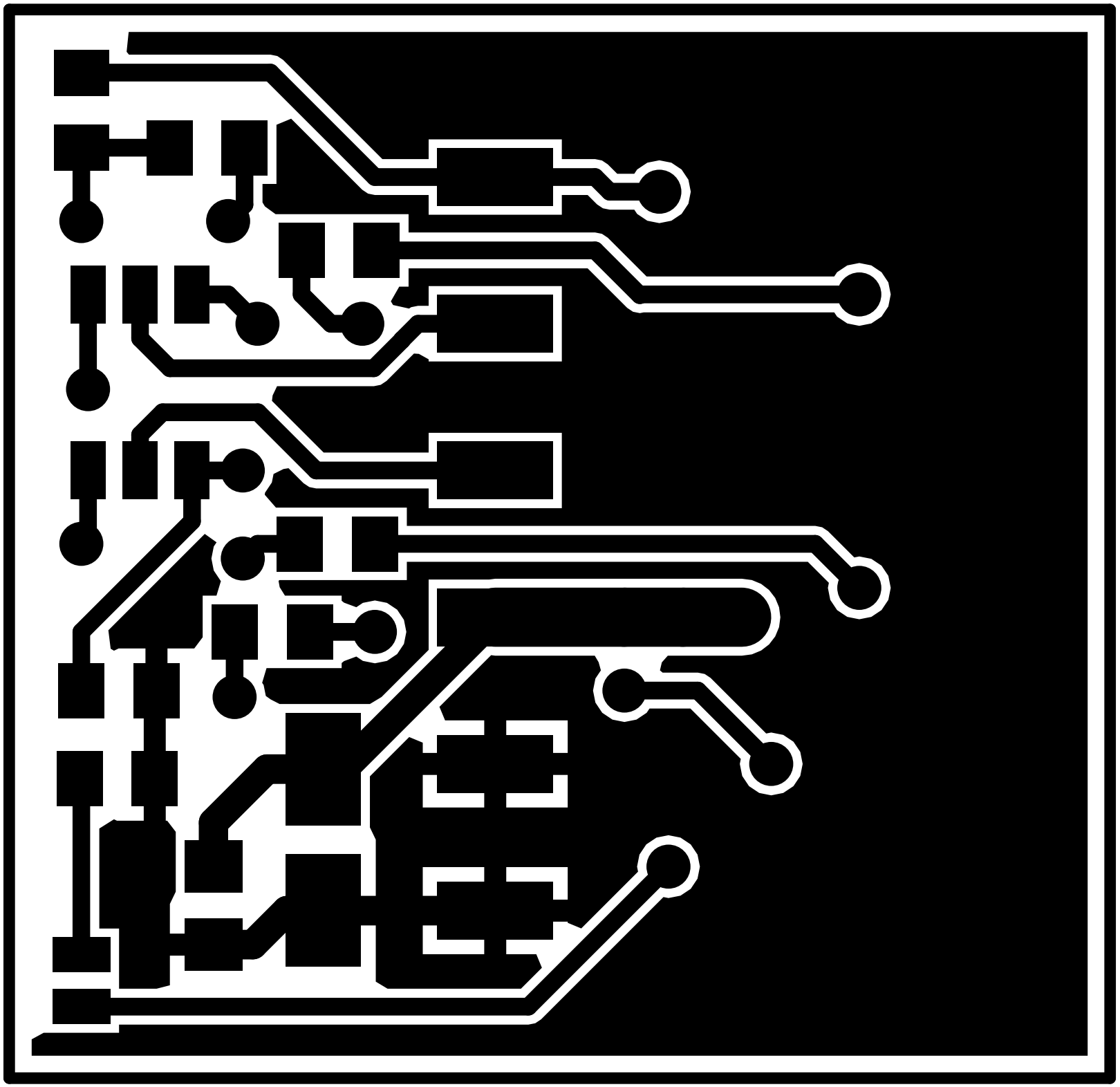
Approved

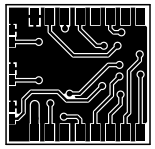
Notes

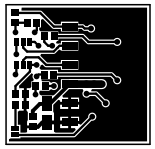

D3
D2
D1
U1


R1
R3
R5
J1
J2
R4
R2
R6
C2
Q1
R7
J3
20160228
P1
ESP2FTDI V1.0









Design Rules Verification Report

Filename : C:\Users\bc547\Documents\bcdev-data\projects\esp2ftdi\hardware\adapterboard.PcbDoc

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Net Antennae (Tolerance=0mil) (All)	0
Silk to Silk (Clearance=5mil) (All),(All)	0
Silk To Solder Mask (Clearance=5mil) (IsPad),(All)	0
Minimum Solder Mask Sliver (Gap=3mil) (All),(All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Hole Size Constraint (Min=13mil) (Max=100mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Width Constraint (Min=10mil) (Max=100mil) (Preferred=10mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Clearance Constraint (Gap=6mil) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Minimum Annular Ring (Minimum=7mil) (All)	0
Board Clearance Constraint (Gap=0mil) (Not OnSilkscreen)	0
Total	0