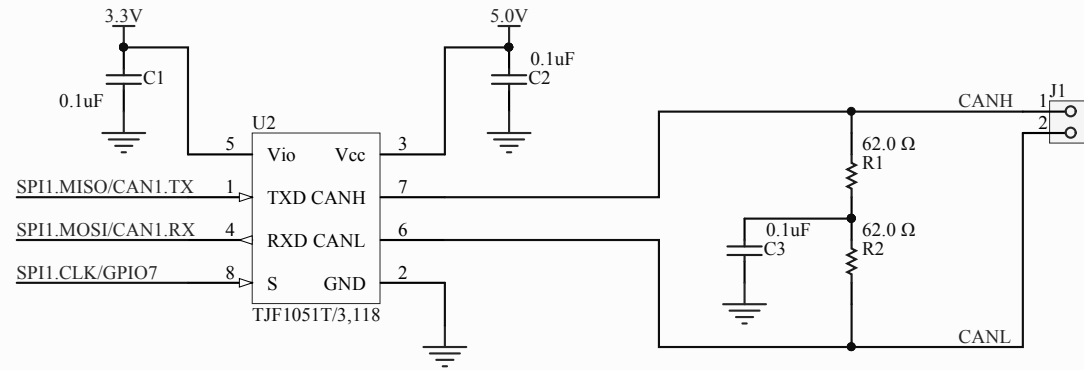
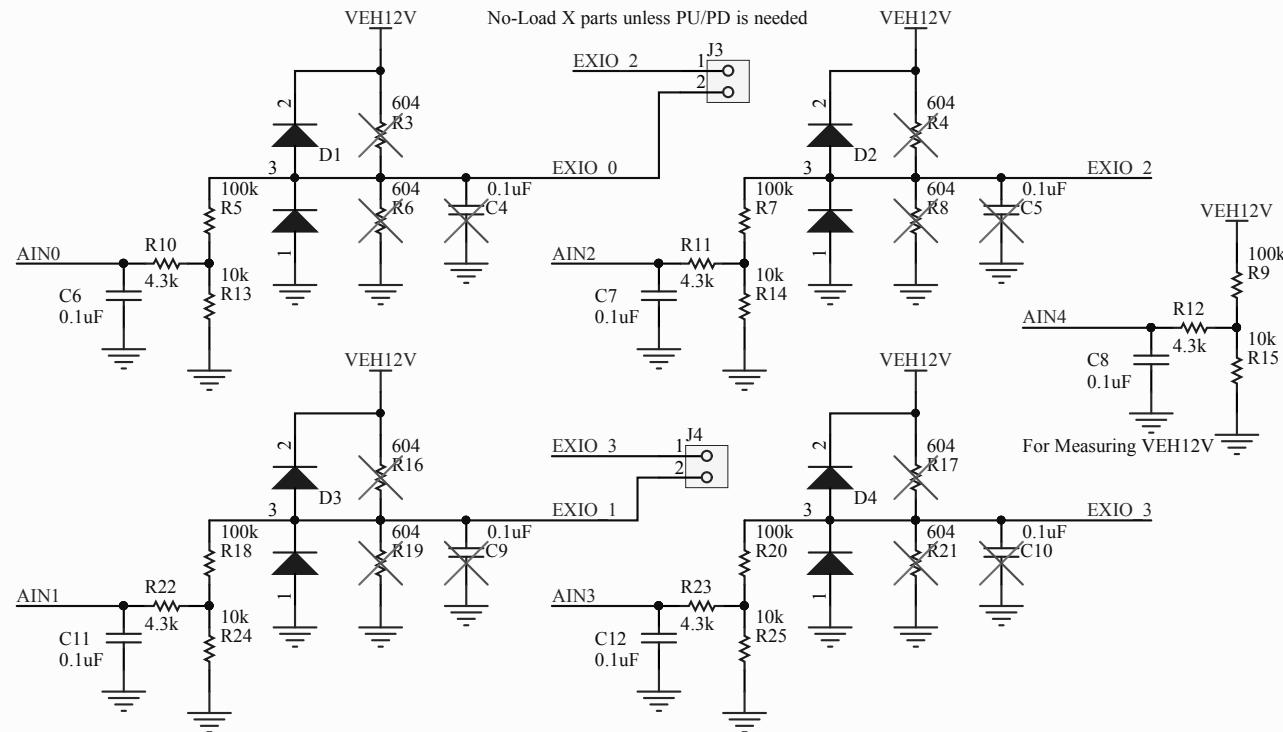


[illegible]

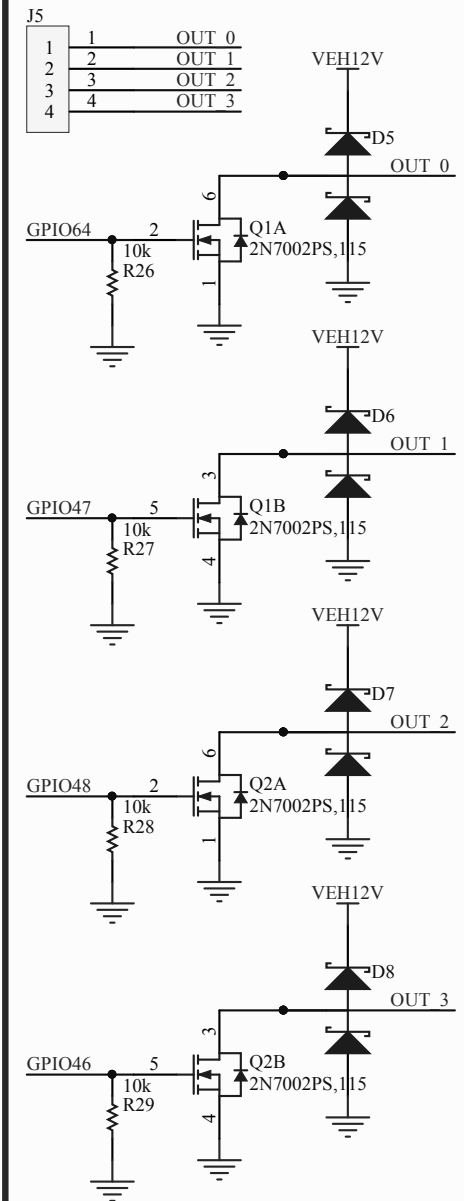
## CAN Tranciever



## Analog Input (Assume VEH12V will not exceed 18V)



## Relay Sink Drivers (Max 1A)



Title

Pocket Beagle Automotive Cape

Size

Number

Revision

1.0

Date: 1/26/2019

Sheet of 2

File: Sheet1.AutomotiveIO.SchDoc

Drawn By: Miller

PocketCape Interface

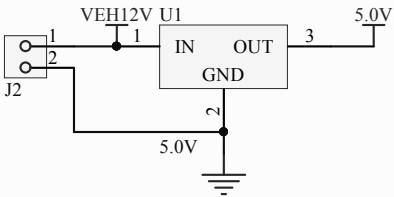
5.0V	P1	1	2	AIN6/GPIO87
USB1.DRVVBUS		3	4	GPIO89
USB1.VBUS		5	6	SPI0.CS
USB1.VIN		7	8	SPI0.CLK
USB1.D-		9	10	SPI0.MISO
USB1.D+		11	12	SPI0.MOSI
USB1.ID		13	14	3.3V
GND		15	16	GND
AIN.VREF-		17	18	AIN.VREF+
AIN0		19	20	GPIO20
AIN1		21	22	GND
AIN2		23	24	VOUT
AIN3		25	26	I2C2.SDA
AIN4		27	28	I2C2.SCL
PRU0.7		29	30	UART0.TX
PRU0.4		31	32	UART0.RX
PRU0.1		33	34	GPIO26
PRU1.10		35	36	PWM0A

FCI 76385-318LF

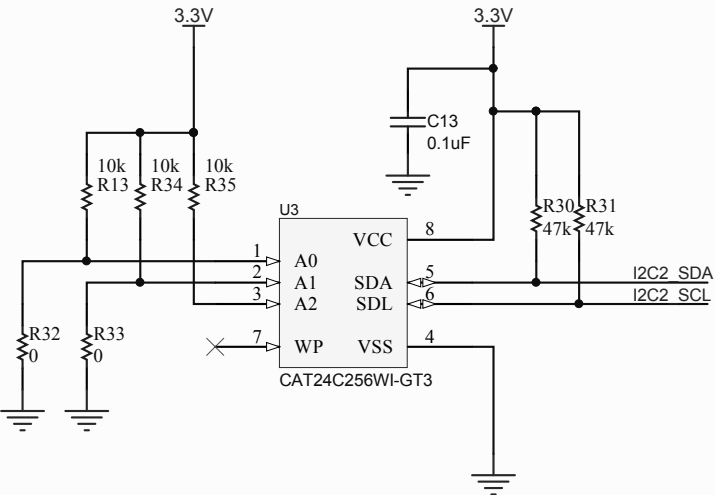
PWM1A	P2	1	2	GPIO59
GPIO23		3	4	GPIO58
UART4.RX		5	6	GPIO57
UART4.TX		7	8	GPIO60
I2C1.SCL		9	10	GPIO52
I2C1.SDA		11	12	PWR.PTN
VOUT		13	14	BAT.VIN
GND		15	16	BAT.TMP
GPIO65		17	18	GPIO47
GPIO27		19	20	GPIO64
GND		21	22	GPIO46
3.3V		23	24	GPIO48
SPI1.MOSI/CAN1.RX		25	26	RESET#
SPI1.MISO/CAN1.TX		27	28	PRU0.6
SPI1.CLK/GPIO7		29	30	PRU0.3
SPI1.CS		31	32	PRU0.2
GPIO45		33	34	PRU0.5
AIN5		35	36	AIN7

FCI 76385-318LF

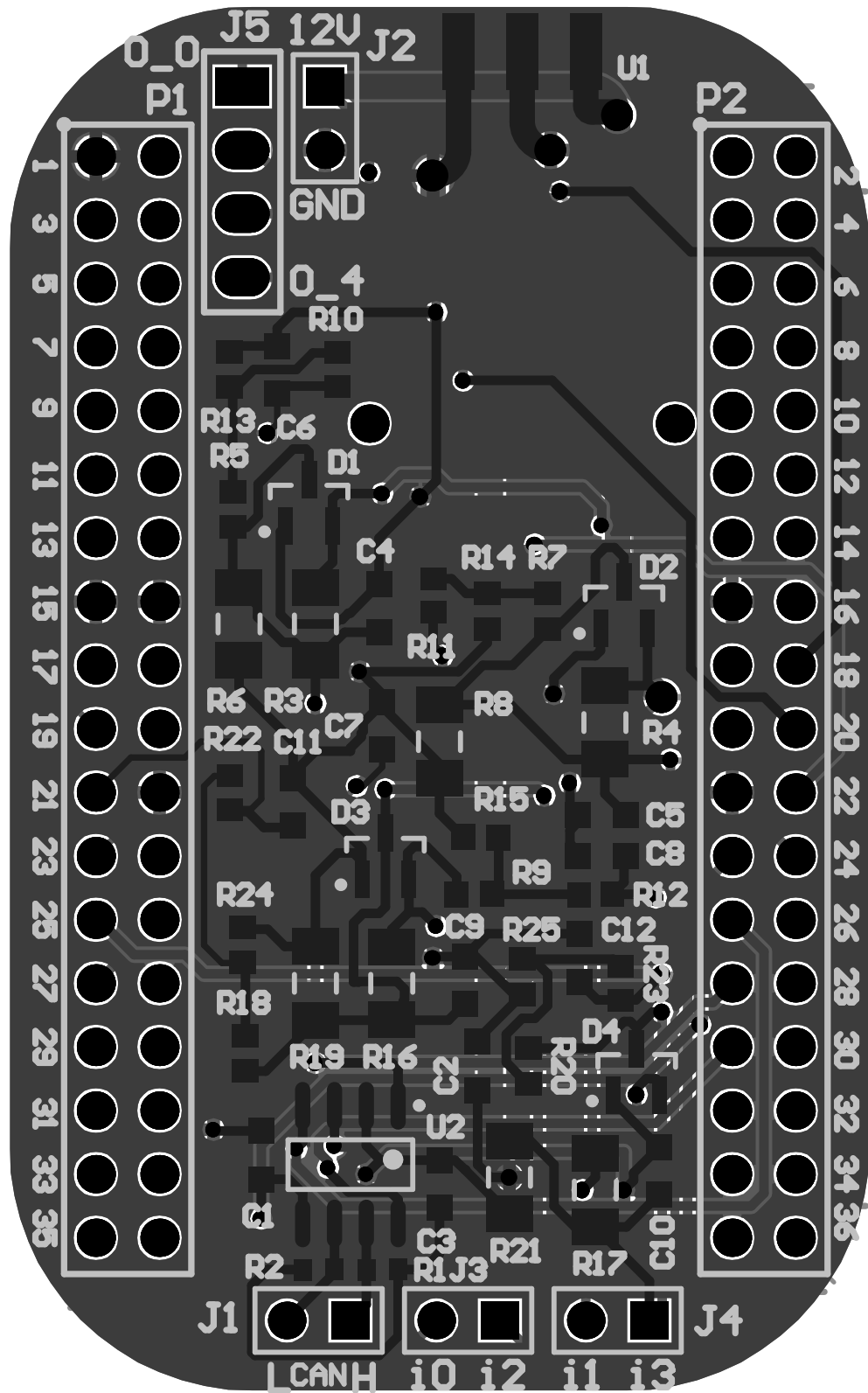
Vehicle Input Power

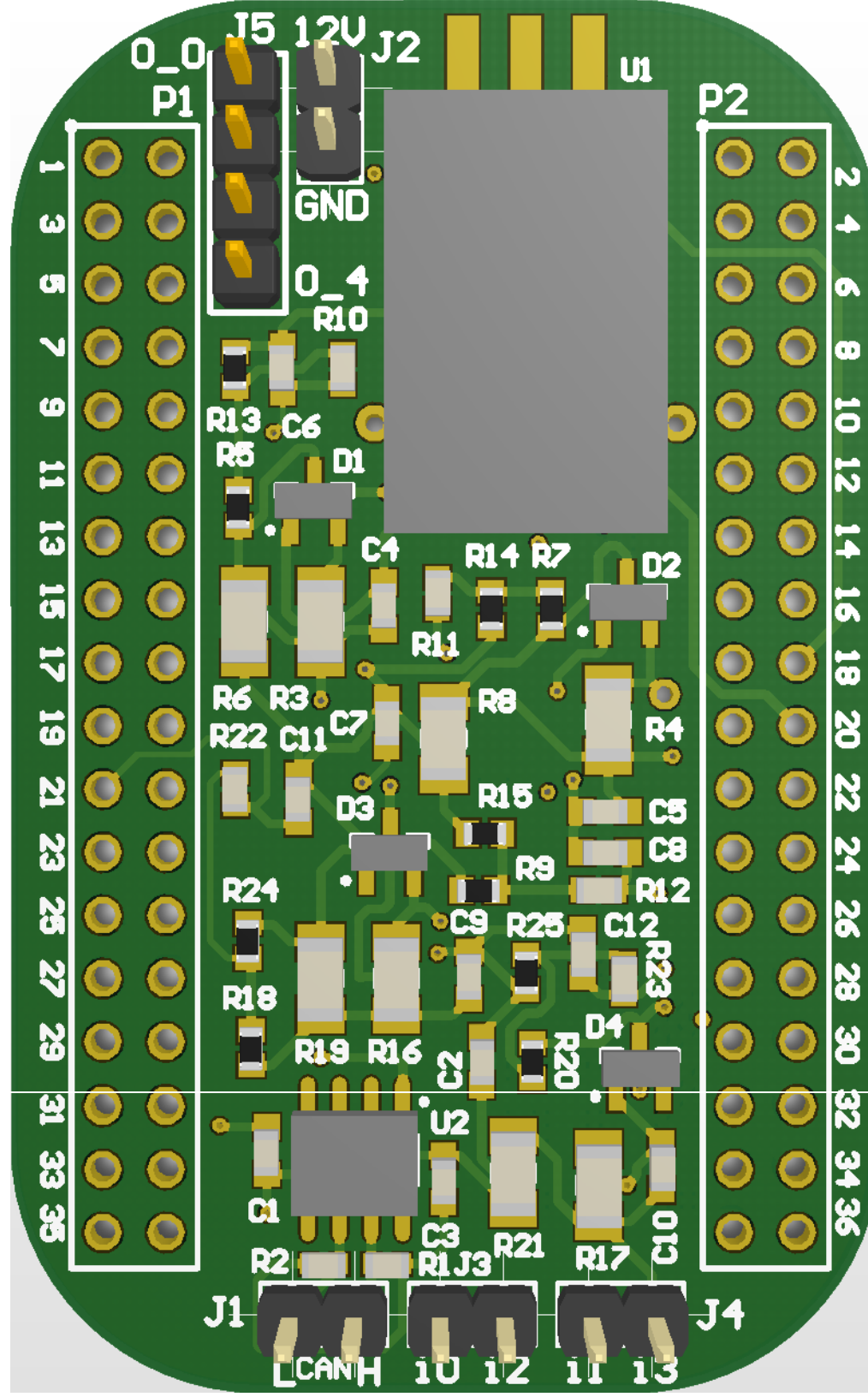


Device Tree Overlay Support ??



Title		
Pocket Beagle Automotive Cape		
Size	Number	Revision
A		1.0
Date:	1/26/2019	Sheet of 2
File:	Sheet1.MainIO.SchDoc	Drawn By: Miller





## Design Rules Verification Report

Filename : C:\ProgramData\Altium\CircuitMaker {E16EADF4-A822-4832-8FAF-288EE79AFA6A}\Projects\E5E36FD3-2CD8-4D85-81A3-8F768E1EFB3F\16cbb6d9-1a7f-4af0-ad25-b1317df75c25\PCB1.CMPcbDoc

Warnings 0  
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Net Antennae (Tolerance=0mil) (All)	0
Clearance Constraint (Gap=5mil) (All),(All)	0
Width Constraint (Min=10mil) (Max=40mil) (Preferred=15mil) (All)	0
Power Plane Connect Rule(Relief Connect )(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ( (All) )	0
Hole Size Constraint (Min=8mil) (Max=100mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Preferred=500mil) (All)	0
Hole T o Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.5mil) (All),(All)	0
Silk To Solder Mask (Clearance=0mil) (IsPad),(All)	0
Silk to Silk (Clearance=1mil) (All),(All)	0
Silk primitive without silk layer	0
Unpoured Polygon (Allow unpoured: False)	0
Total	0