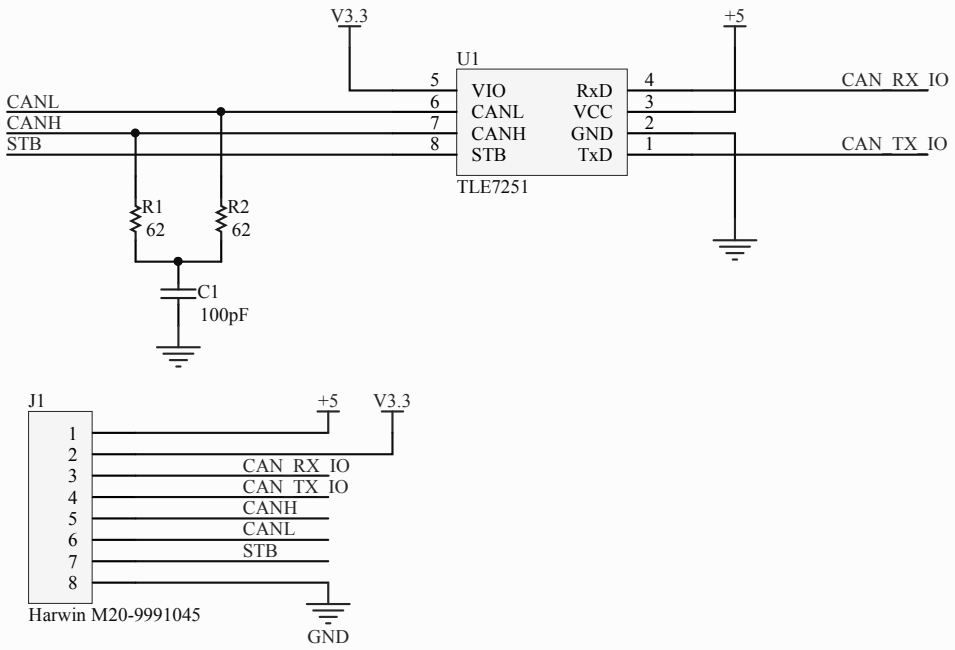
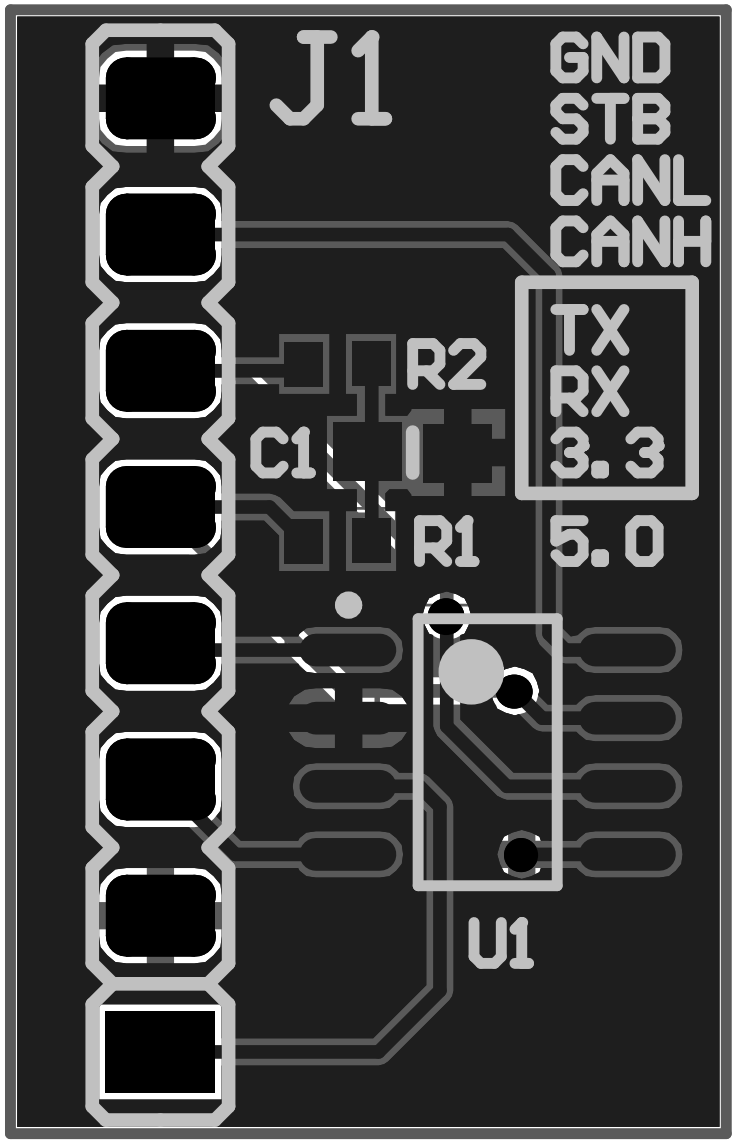


Title		
Size: A	Number	Revision
Date: 4/12/2019		Sheet of
File: Sheet1.SchDoc		Drawn By:


J1
GND
STB
CANL
CANH
TX
RX
3.3
5.0
R2
C1
R1
U1

Comment	Description	Designator	Footprint	LibRef	Quantity
AVX 06035A101JAT2A	0603 100 pF 50 V ±5% Tol. C0G/NP0 Surface Mount Multilayer Ceramic Capacitor	C1	CAPC1608X90X35ML15T15	CMP-4aa080e74f2e9567-1	1
Harwin M20-9991045	Header Connector, PCB Mount, RECEPT, 8 Contacts, PIN, 0.1 Pitch, R ANGLE PC TAIL Terminal	J1	PCB-5069yp845a99ca3lzjl2-1	CMP-967a5f748d4649bd-3	1
Panasonic ERJ-3GEYJ620V	Thick Film Resistors - SMD 0603 62ohms 5% Tol	R1, R2	RESC1608X55X30LL15T15	CMP-3651708-2	2
Infineon TLE7251VSJXUM	Integrated circuit: transc	U1	PCB-vqo562b3a5tq4gh3	CMP-3c1cf6ff8d9fe3db-1	1

Design Rules Verification Report

Filename : C:\ProgramData\Altium\CircuitMaker {5028051A-F9E3-4B0C-A31C-394BA9628B02}\Projects\E5E36FD3-2CD8-4D85-81A3-8F768E1EFB3F\6f92f8d3-3c1c-42fa-bbc2-ded2b46cb8fb\PCB1.CMPcbDoc

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Unpoured Polygon (Allow unpoured: False)	0
Silk primitive without silk layer	0
Silk to Silk (Clearance=5mil) (All),(All)	0
Silk To Solder Mask (Clearance=1mil) (IsPad),(All)	0
Minimum Solder Mask Sliver (Gap=1mil) (All),(All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Hole Size Constraint (Min=8mil) (Max=100mil) (All)	0
Un-Routed Net Constraint ((All))	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Width Constraint (Min=5mil) (Max=60mil) (Preferred=10mil) (All)	0
Clearance Constraint (Gap=5mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Total	0

Electrical Rules Check Report

Class	Document	Message
Warning	Sheet1.SchDoc	Part J1 is not linked to Octopart