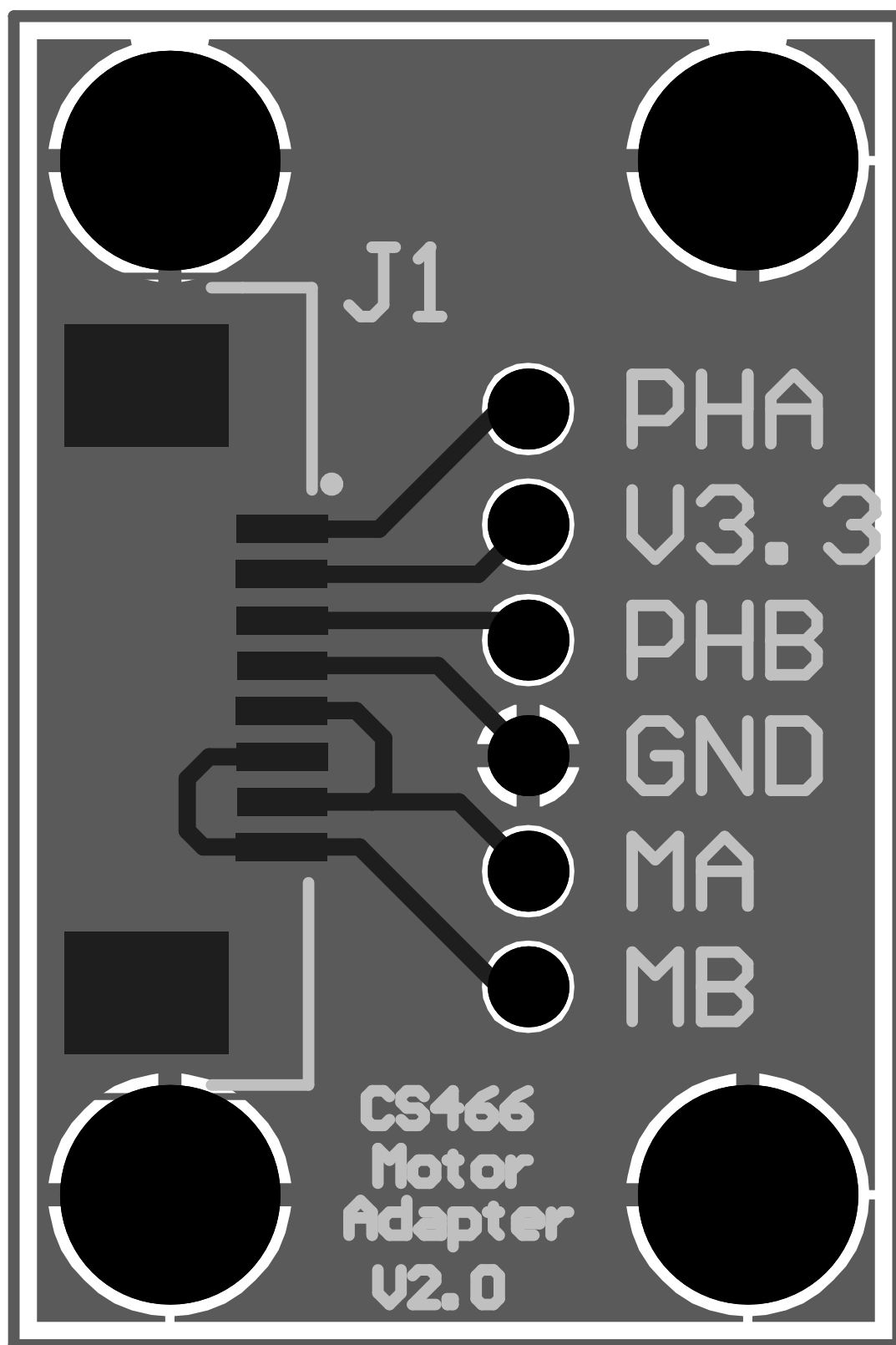
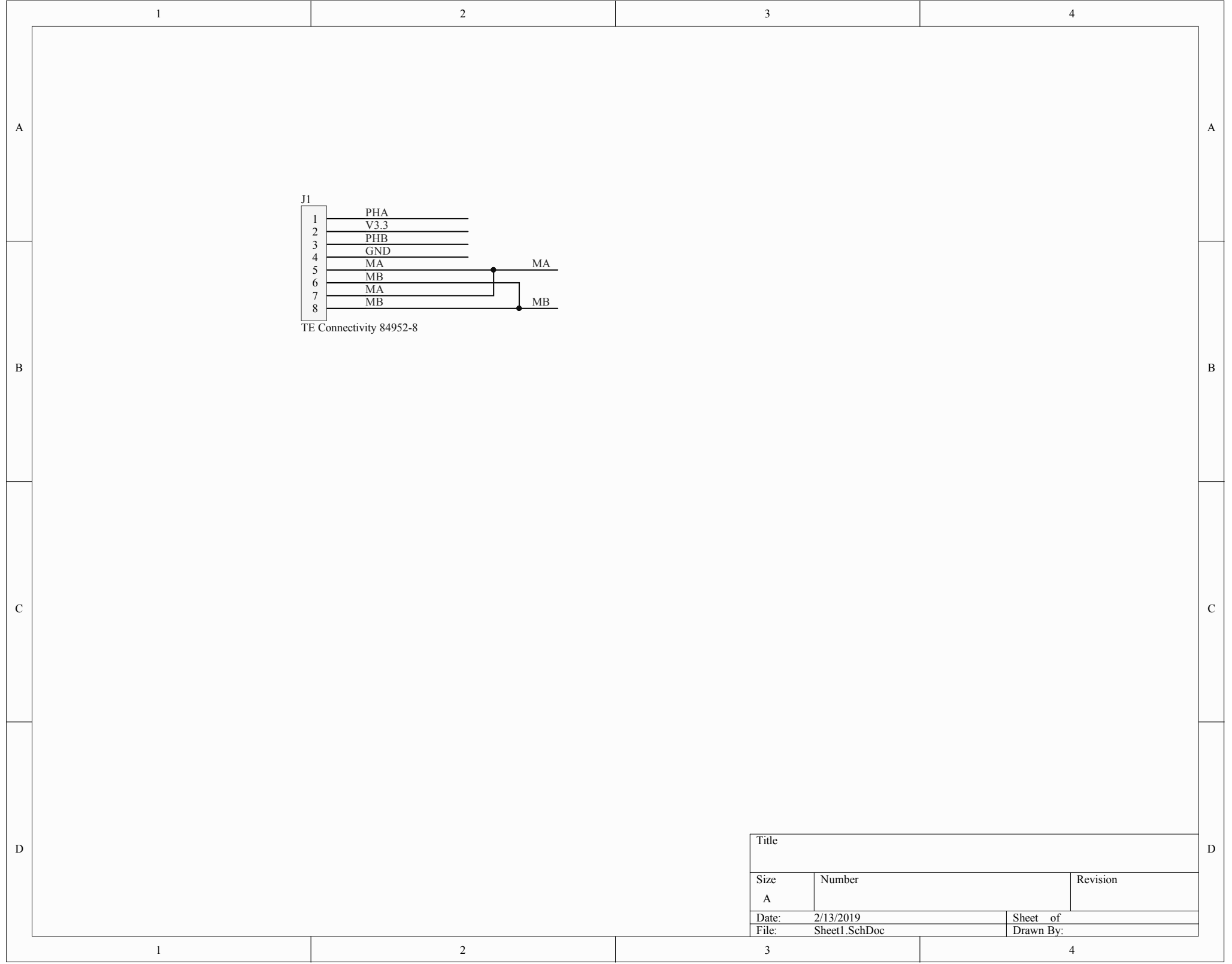


Comment	Description	Designator	Footprint	LibRef	Quantity
TE Connectivity 84952	FFC / FPC Board Conn	J1	PCB-0pts0pyf1xu94m	CMP-3e83f5edd02fe1	1





Title		
Size	Number	Revision
A		
Date:	2/13/2019	Sheet of
File:	Sheet1.SchDoc	Drawn By:

Design Rules Verification Report

Filename : C:\ProgramData\Altium\CircuitMaker {E16EADF4-A822-4832-8FAF-288EE79AFA6A}\Projects\E5E36FD3-2CD8-4D85-81A3-8F768E1EFB3F\dcf17563-8632-43f9-b544-45b3be6dfb9f\PCB1.CMPcbDoc

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Unpoured Polygon (Allow unpoured: False)	0
Silk primitive without silk layer	0
Silk to Silk (Clearance=5mil) (All),(All)	0
Silk To Solder Mask (Clearance=1mil) (IsPad),(All)	0
Minimum Solder Mask Sliver (Gap=1mil) (All),(All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Preferred=500mil) (All)	0
Hole Size Constraint (Min=10mil) (Max=265mil) (All)	0
Un-Routed Net Constraint ((All))	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Width Constraint (Min=10mil) (Max=40mil) (Preferred=15mil) (All)	0
Clearance Constraint (Gap=5mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Total	0