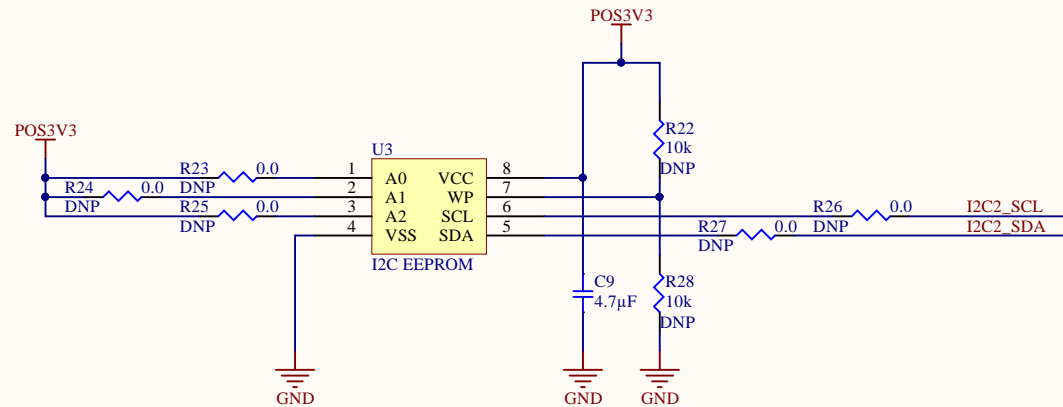
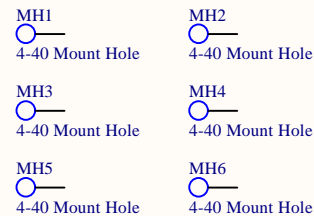


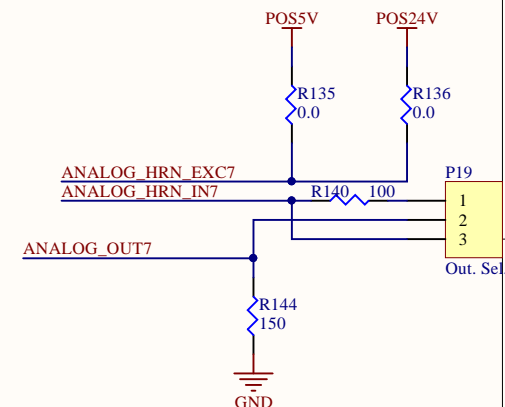
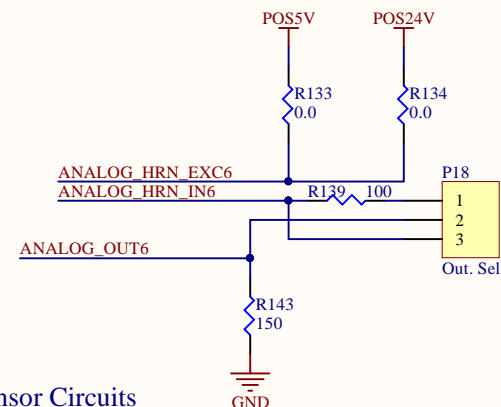
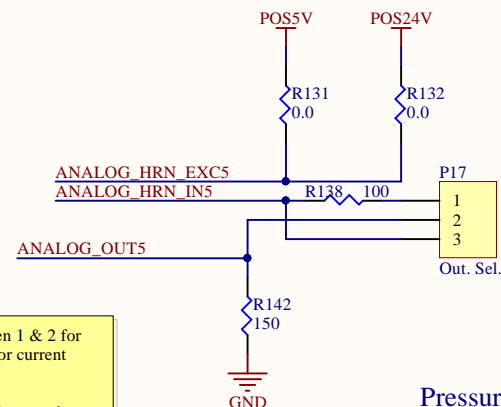
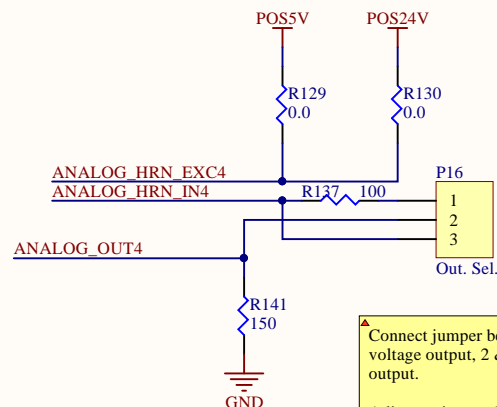
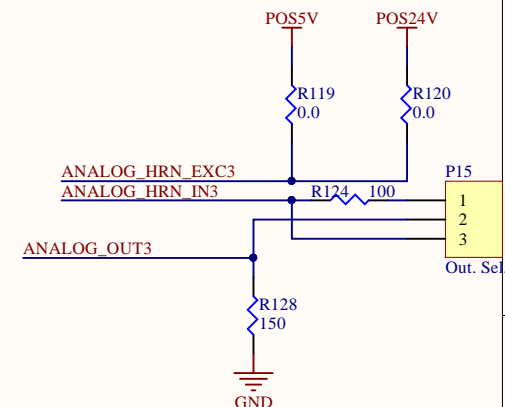
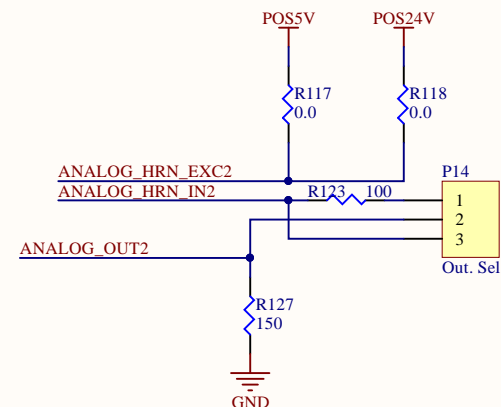
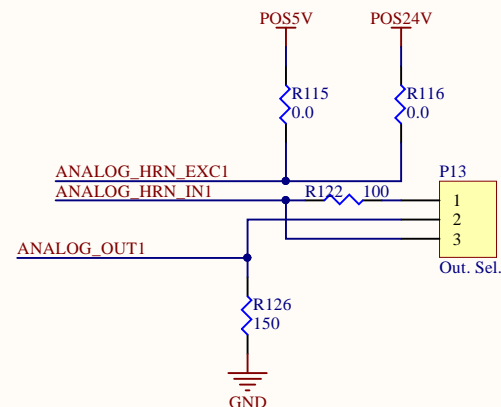
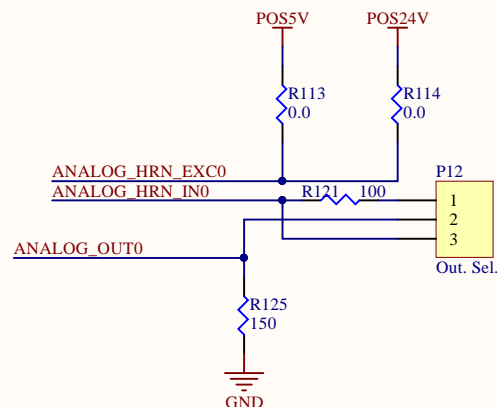
Main Connector



I2C EEPROM



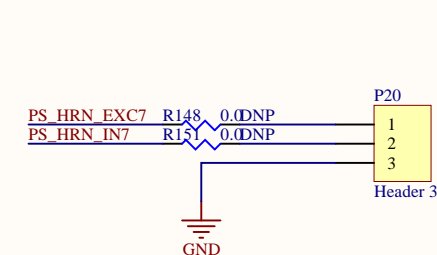
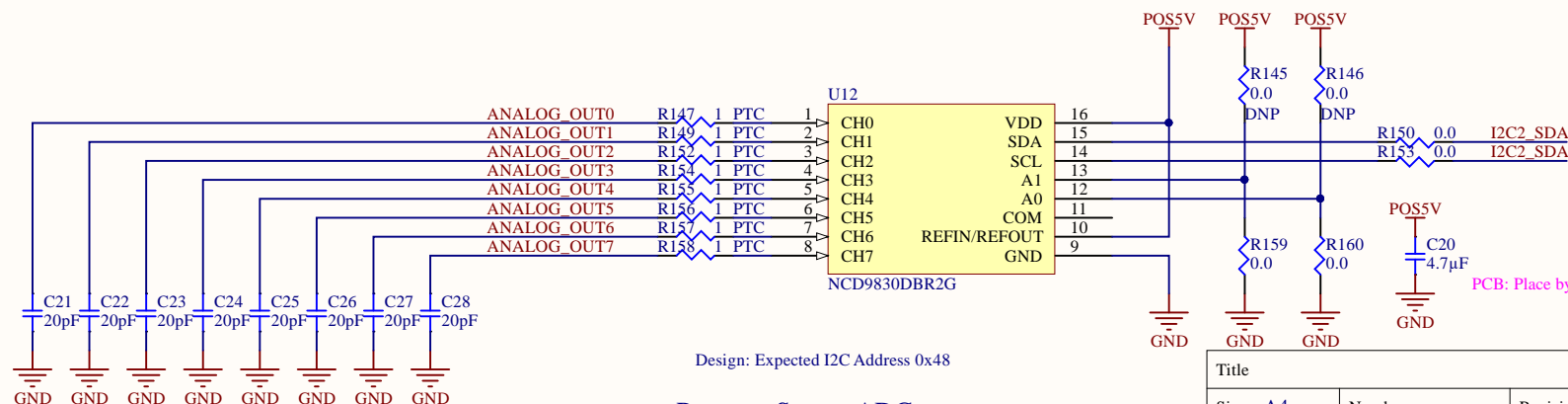
MECHANICAL



Connect jumper between 1 & 2 for voltage output, 2 & 3 for current output.

Adjust resistor values for actual sensor output

## Pressure Sensor Circuits




PCB: Place bypass cap near ADC

Testing: Connect PS directly to P?

Design: Expected I2C Address 0x48

## Pressure Sensor ADC

PCB: Place debouncing caps near ADC

Title			<i>Badgerloop</i> 133 Engineering Research Building Madison, WI 53715	
Size: <b>A4</b>	Number:	Revision:		
Date: <b>1/21/2019</b>	Time: <b>9:29:57 PM</b>	Sheet <b>of</b>		
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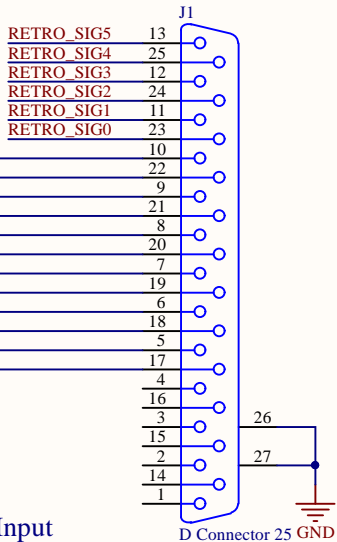
**BADGER**  
**LOOP**

BROWN: 24V  
BLUE: GND  
BLACK: SIG

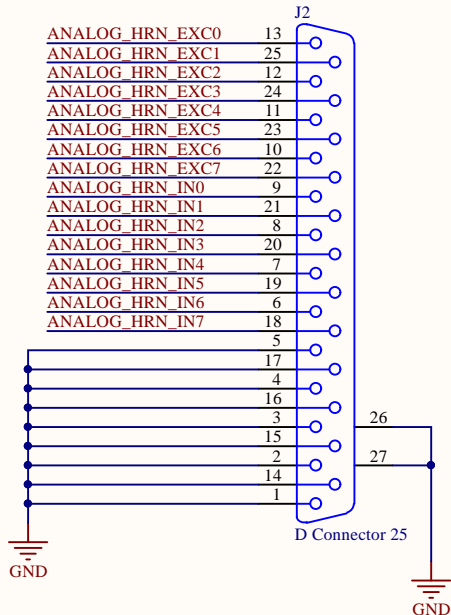
POS24V

GND

Retroreflective Sensor Input

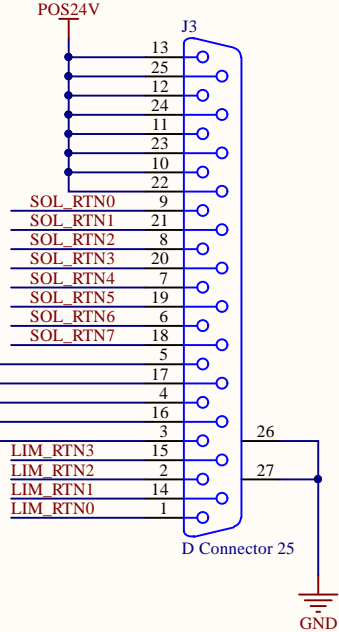


Generic Analog Input

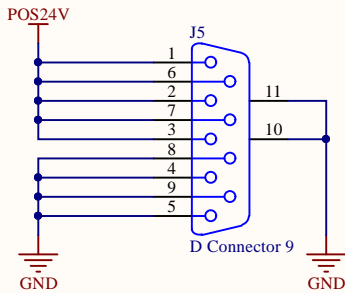


POS5V

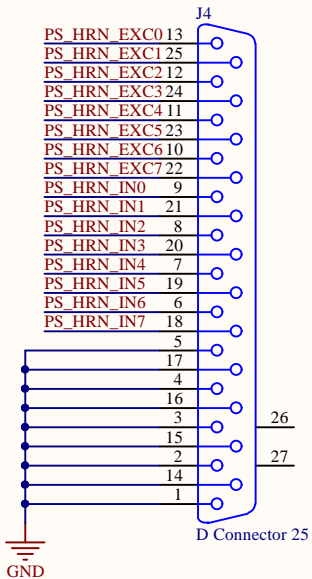
GND



24V PWR

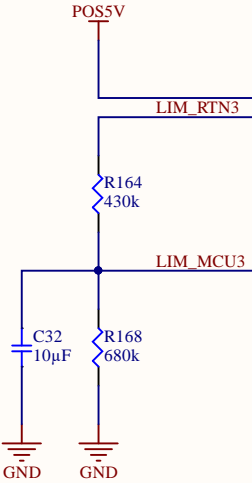
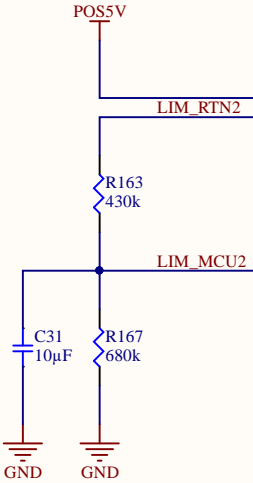
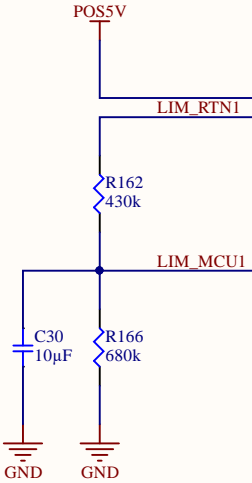
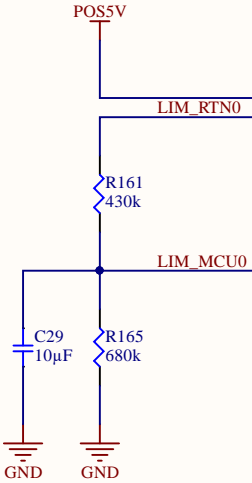


Pressure Sensor Input

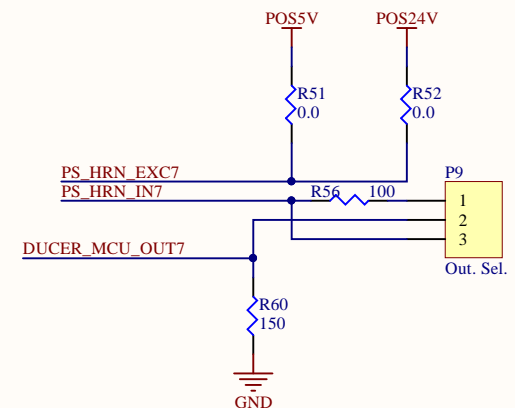
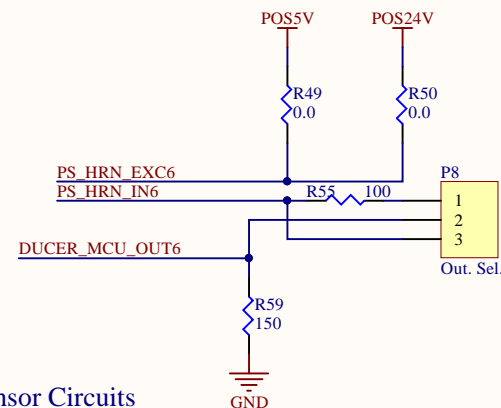
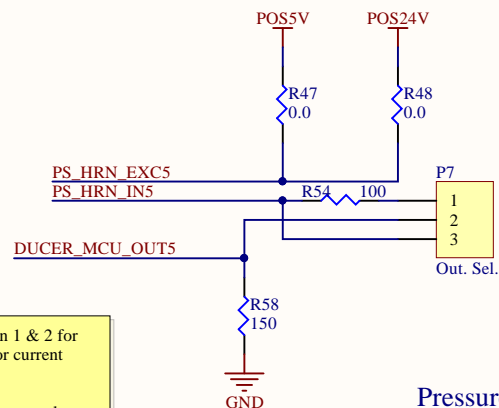
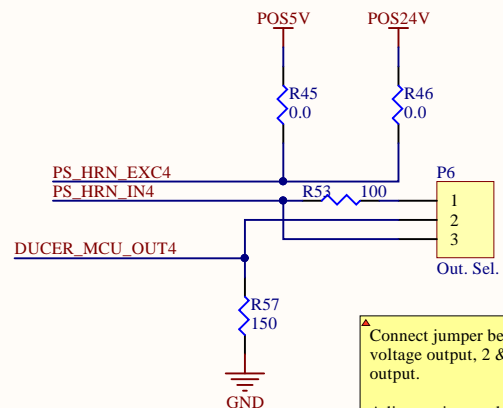
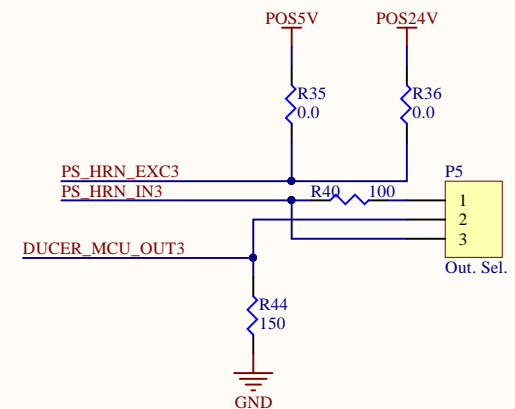
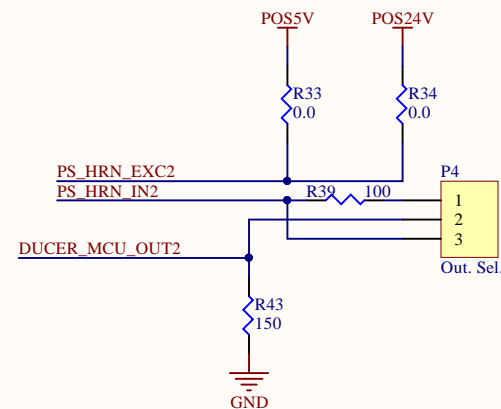
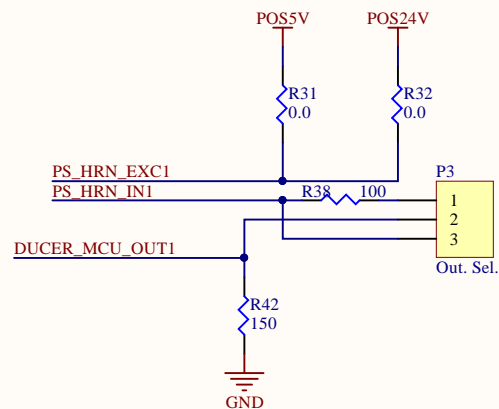
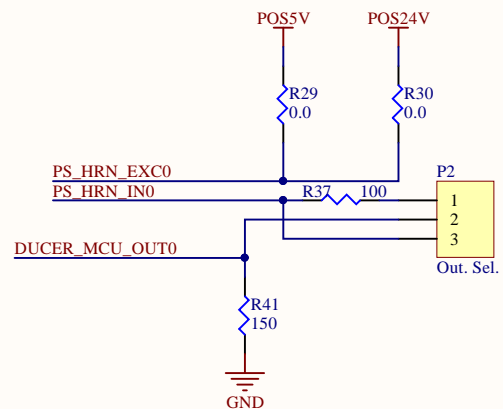




$$f_c = \frac{1}{2\pi*(R_1//R_2)*C_1}$$
  
 $f_c = 60.4\text{Hz}$

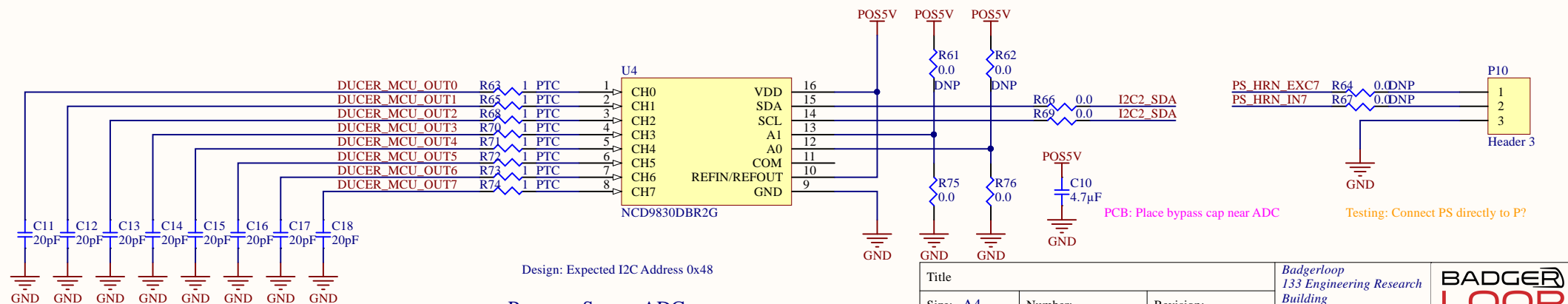


Limit Switch Inputs



- Connect jumper between 1 & 2 for voltage output, 2 & 3 for current output.
- Adjust resistor values for actual sensor output

## Pressure Sensor Circuits



PCB: Place debouncing caps near ADC

## Pressure Sensor ADC

Design: Expected I2C Address 0x48

Title		
Size: <a href="#">A4</a>	Number:	Revision:
Date: <a href="#">1/21/2019</a>	Time: <a href="#">9:29:58 PM</a>	Sheet of
File: <a href="#">C:\git\ fifth\podiv-altium\src\prj\sch\lv_io_pressure.SchDoc</a>		

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Building  
Madison, WI 53715*

**BADGER<sup>®</sup>**  
**LOOP**

Testing: Connect PS directly to P?

A

A

B

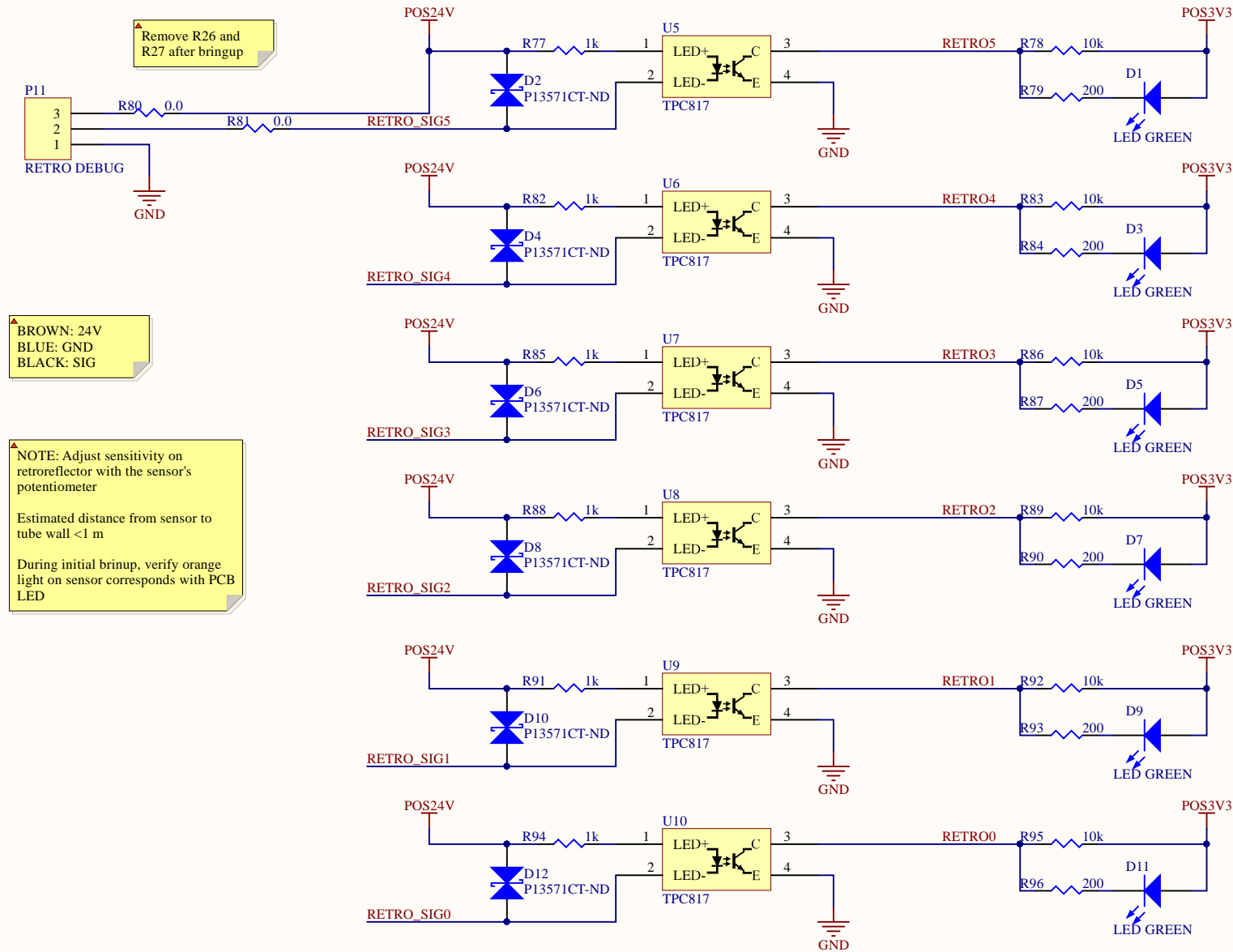
B

C

C

D

D



BROWN: 24V  
BLUE: GND  
BLACK: SIG

NOTE: Adjust sensitivity on retroreflector with the sensor's potentiometer

Estimated distance from sensor to tube wall <1 m

During initial bringup, verify orange light on sensor corresponds with PCB LED


Tape Strip Monitoring:  
RETROS 0-2

Wheel Speed Monitoring:  
RETROS 3-5

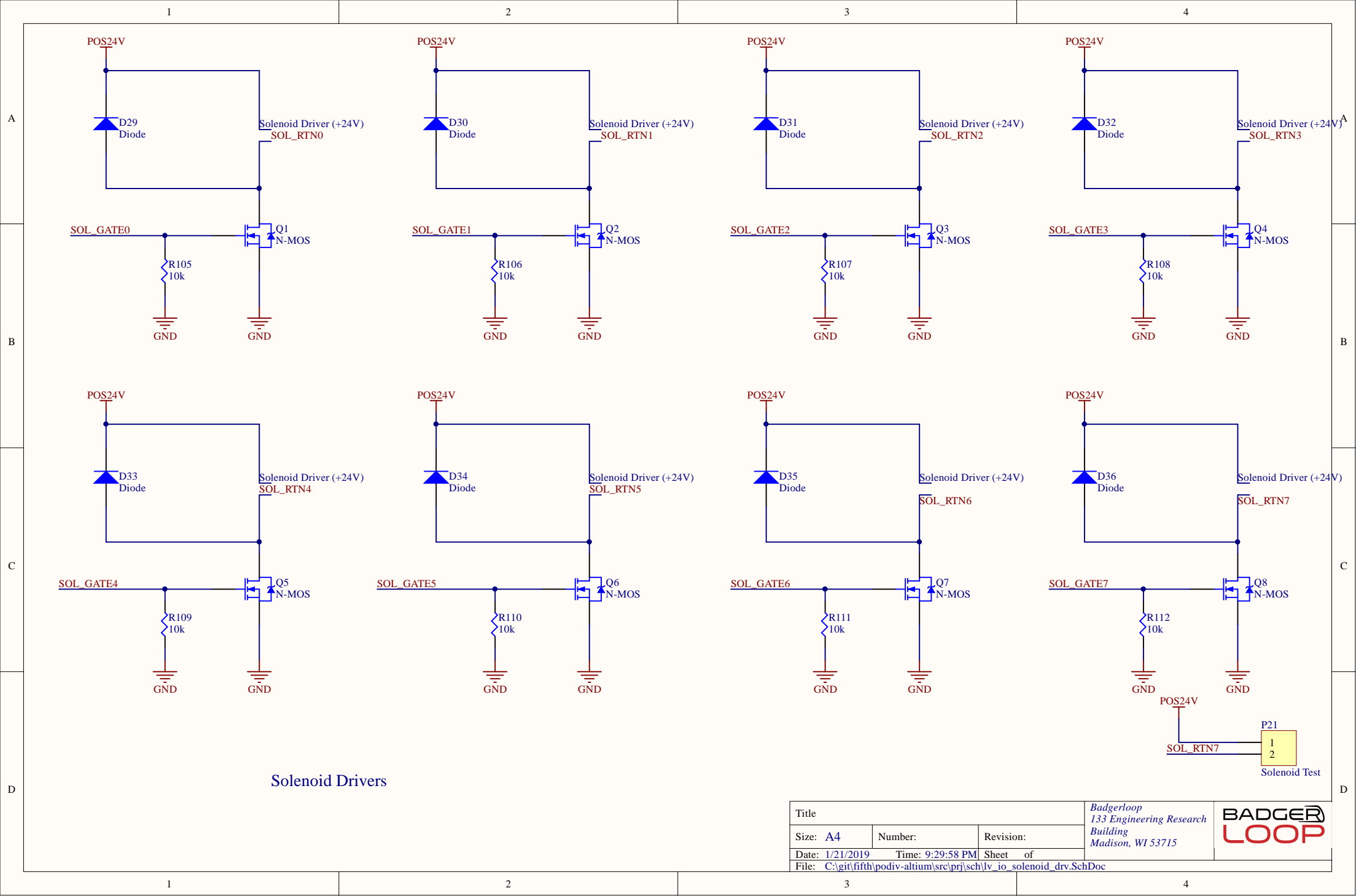


OMIC-0N-0A Photoelectric / Retroreflective Sensor

## Retro Circuits

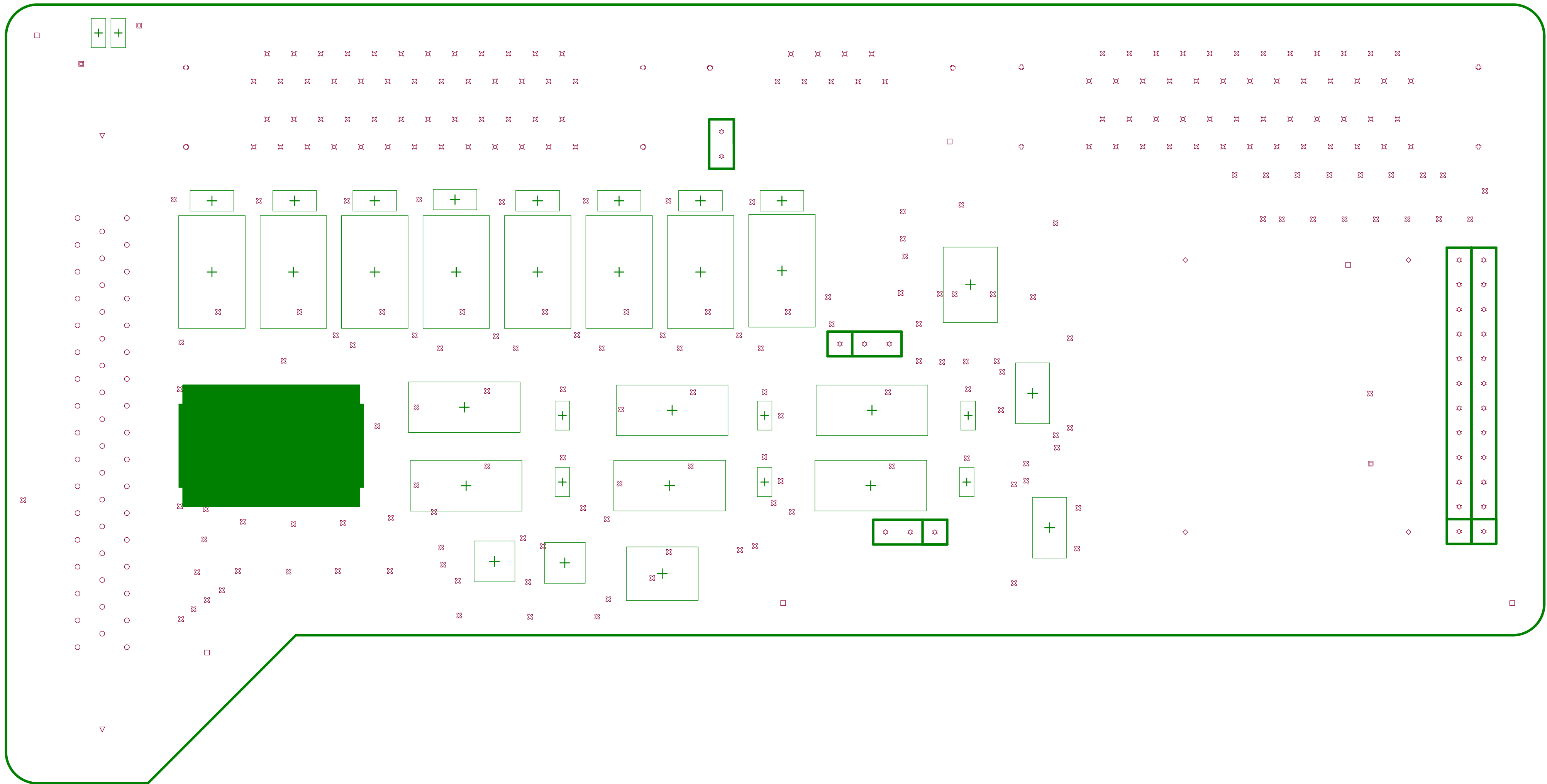
Title			<i>Badgerloop</i> <i>133 Engineering Research</i> <i>Building</i> <i>Madison, WI 53715</i>	
Size: <b>A4</b>	Number:	Revision:		
Date: 1/21/2019	Time: 9:29:58 PM	Sheet of		
File: C:\git\ fifth\podiv-altium\src\prj\sch\lv_io_retro.SchDoc				





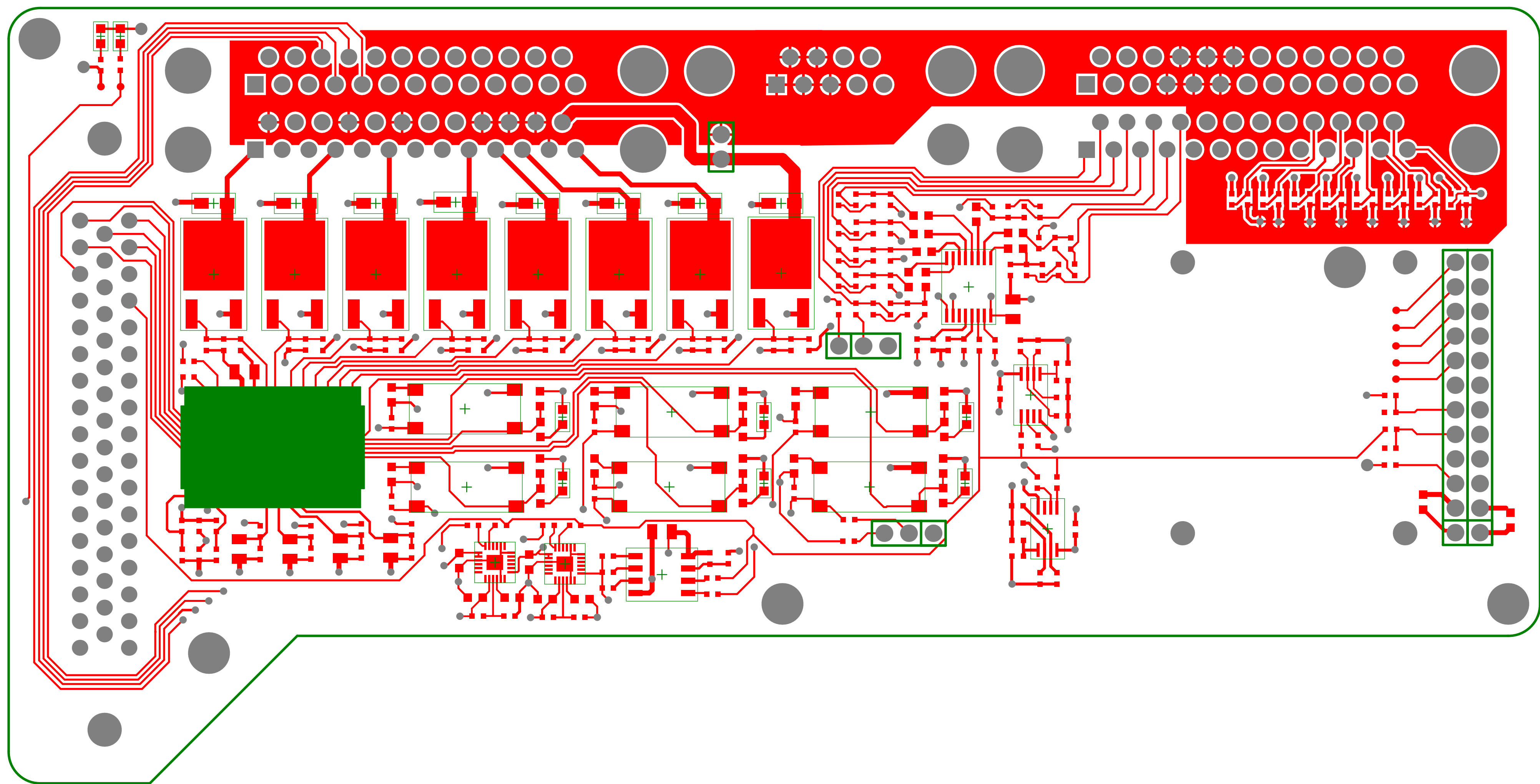
Symbol	Count	Hole Size	Plated	Hole Type	Via/Pad
⌘	135	10.00mil (0.254mm)	PTH	Round	Via
▣	3	28.00mil (0.711mm)	PTH	Round	Via
☆	32	39.37mil (1.000mm)	PTH	Round	Pad
✕	109	42.91mil (1.090mm)	PTH	Round	Pad
○	50	43.31mil (1.100mm)	PTH	Round	Pad
◇	4	78.74mil (2.000mm)	PTH	Round	Pad
□	6	102.36mil (2.600mm)	NPTH	Round	Pad
▽	2	122.05mil (3.100mm)	PTH	Round	Pad
⊕	10	128.35mil (3.260mm)	PTH	Round	Pad
	351 Total				

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
1	Top Overlay								
2	Top Solder	Solder Resist	0.40mil	3.5					
3	Top Layer	Copper	1.40mil						
4	Dielectric 1	FR-4	10.00mil	4.2					
5	GND	Copper	1.42mil						
6	Dielectric 3		5.00mil	4.2					
7	PWR	Copper	1.42mil						
8	Dielectric 2		10.00mil	4.2					
9	Bottom Layer	Copper	1.40mil						
10	Bottom Solder	Solder Resist	0.40mil	3.5					
11	Bottom Overlay								



1. PCB must be 0.030" thick +/- 10%
2. Board Size:
3. Electrical Test
4. Coloring:
  - a. Green Solder Mask Top
  - b. Green Solder Mask Bottom
  - c. White Silkscreen Top
  - d. White Silkscreen Bottom
5. Via annular ring clearance is 10mil minimum
6. Vias are to be covered by soldermask (tented)  
Components with throughholes are P1, J1, J2, J6, P2, P10, P21, MH1-MH6  
All other holes are Vias

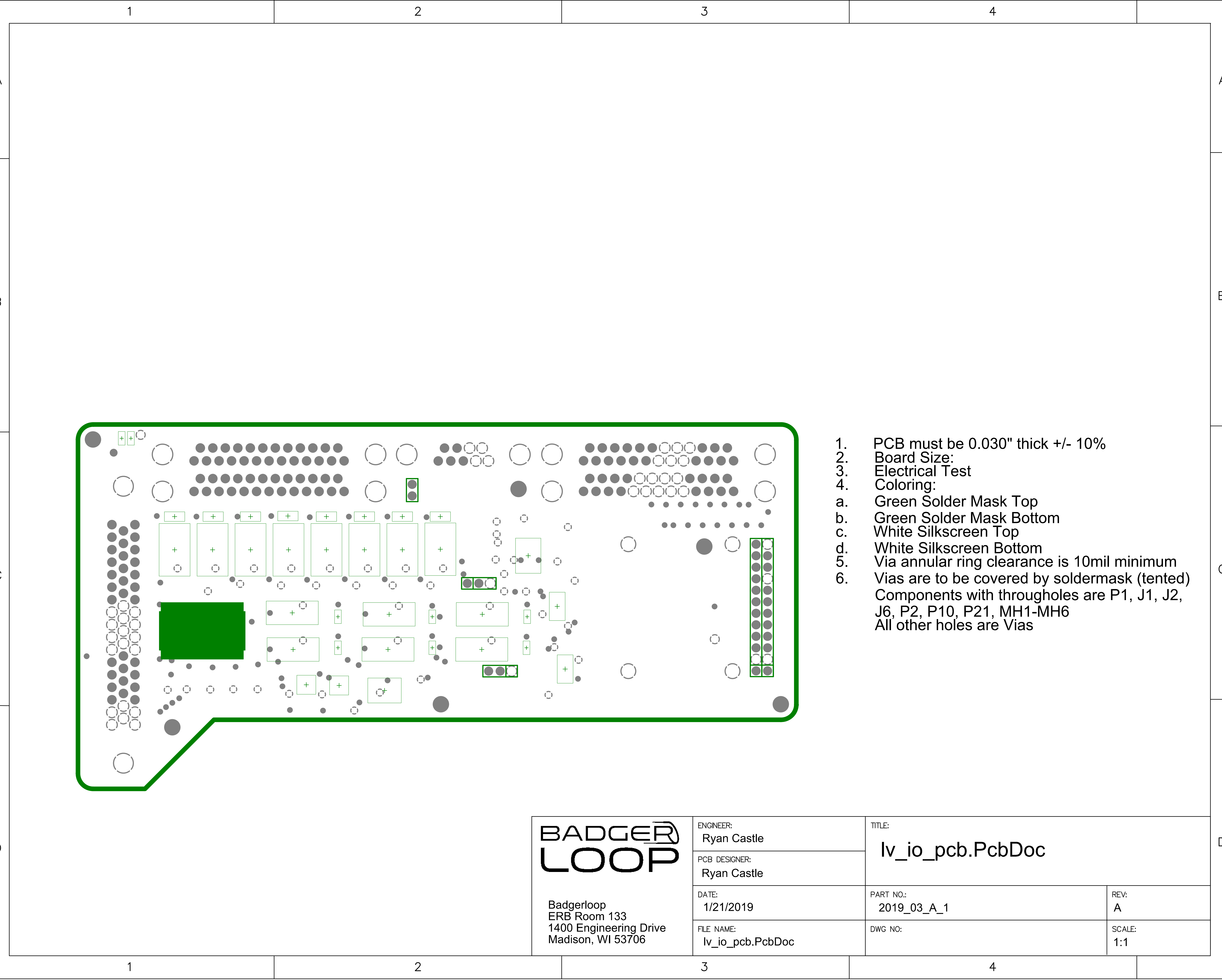
<div>BADGER LOOP</div> <div>Badgerloop ERB Room 133 1400 Engineering Drive Madison, WI 53706</div>	ENGINEER: Ryan Castle	TITLE:  lv_io_pcb.PcbDoc	
	PCB DESIGNER: Ryan Castle		
	DATE: 1/21/2019	PART NO.: 2019_03_A_1	REV: A
	FILE NAME: lv_io_pcb.PcbDoc	DWG NO:	SCALE: 1:1



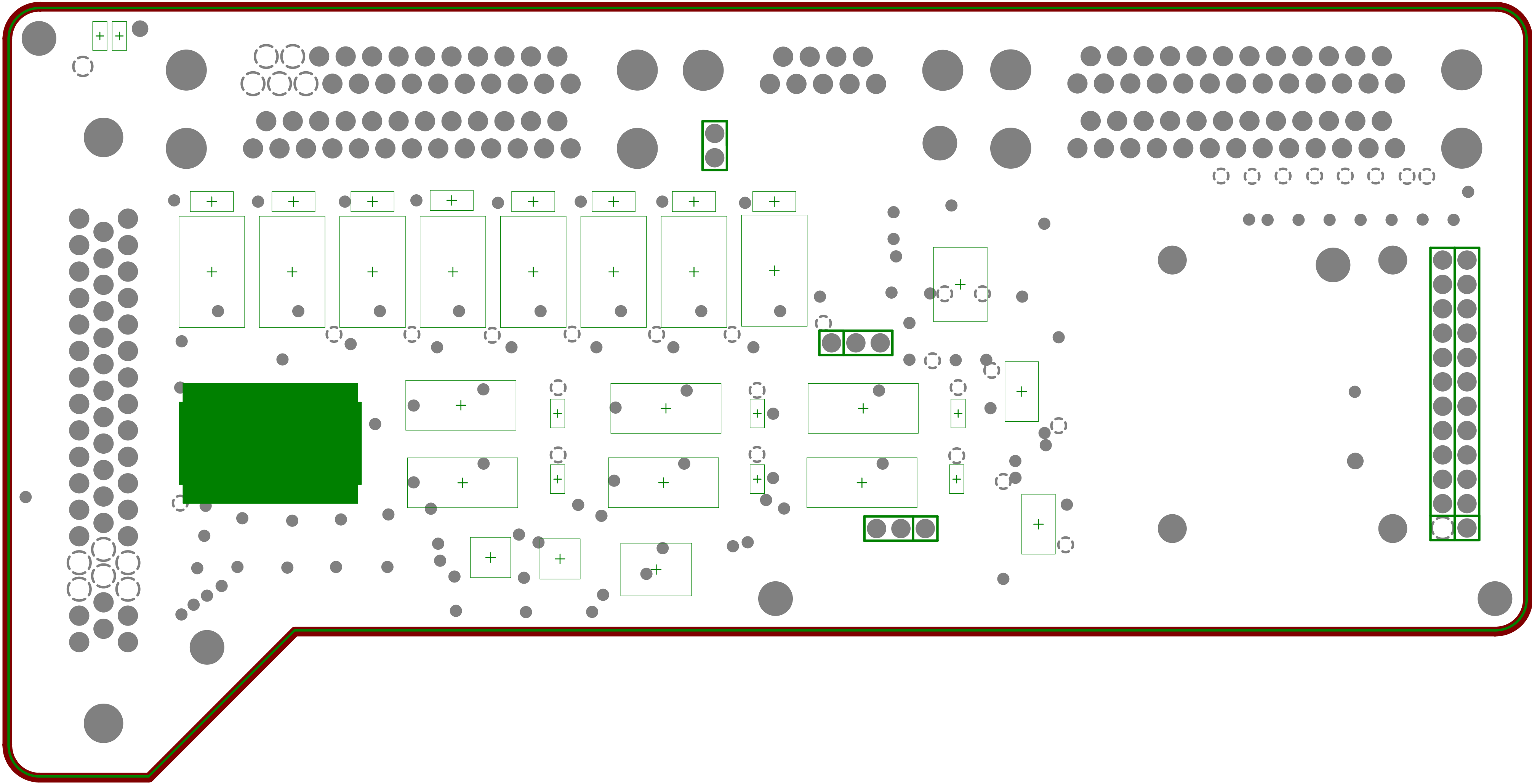
- 1. PCB must be 0.030" thick +/- 10%
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<div><div>BADGER LOOP</div><div>Badgerloop ERB Room 133 1400 Engineering Drive Madison, WI 53706</div></div>	ENGINEER: Ryan Castle	TITLE:  lv_io_pcb.PcbDoc	
	PCB DESIGNER: Ryan Castle		
	DATE: 1/21/2019	PART NO.: 2019_03_A_1	REV: A
	FILE NAME: lv_io_pcb.PcbDoc	DWG NO:	SCALE: 1:1



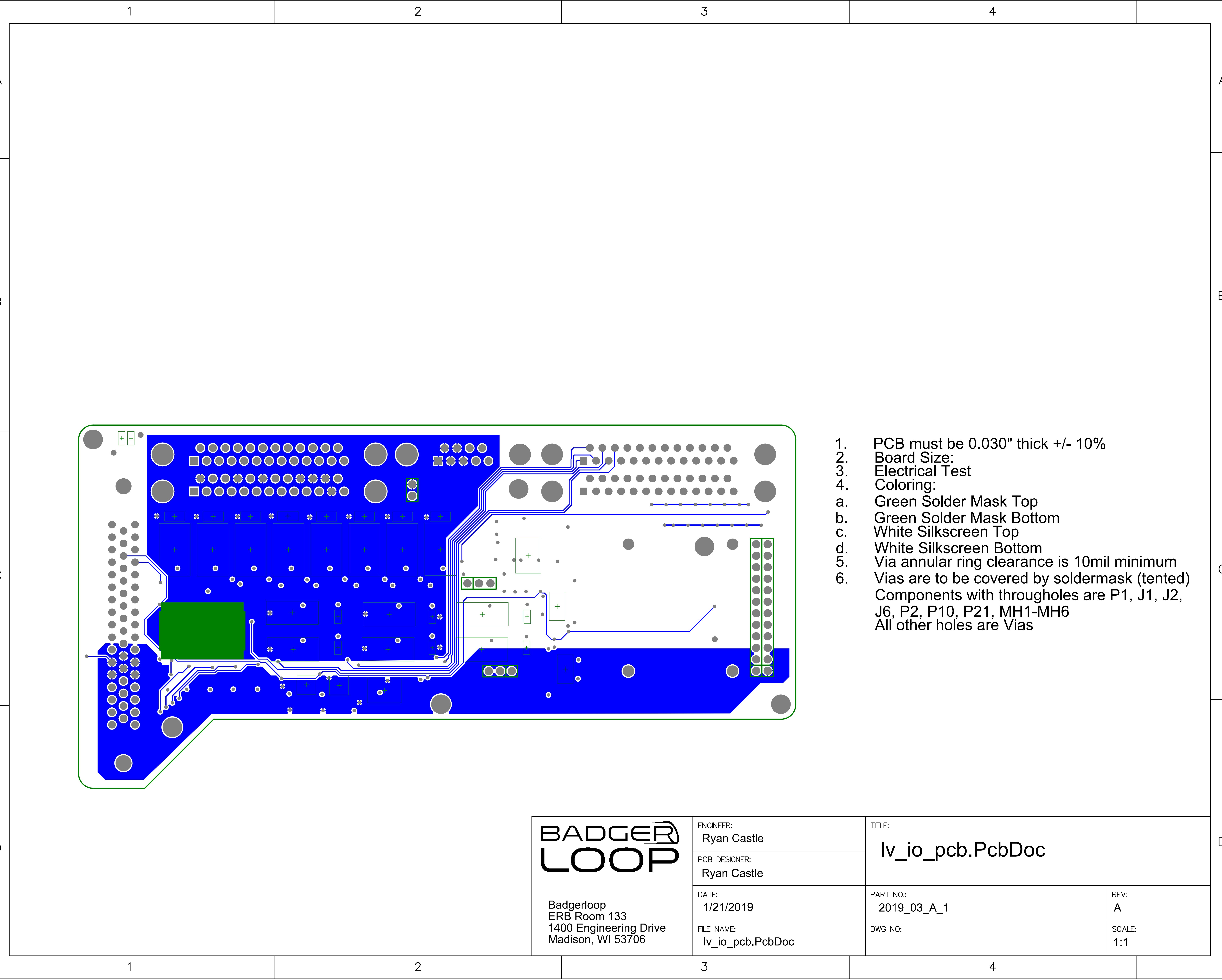






- 1. PCB must be 0.030" thick +/- 10%
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- 3. Electrical Test
- 4. Coloring:
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<div><div>BADGER LOOP</div><div>Badgerloop ERB Room 133 1400 Engineering Drive Madison, WI 53706</div></div>	ENGINEER: Ryan Castle		TITLE:  lv_io_pcb.PcbDoc		
	PCB DESIGNER: Ryan Castle				
	DATE: 1/21/2019		PART NO.: 2019_03_A_1		REV: A
	FILE NAME: lv_io_pcb.PcbDoc		DWG NO:		SCALE: 1:1



- 1. PCB must be 0.030" thick +/- 10%
- 2. Board Size:
- 3. Electrical Test
- 4. Coloring:
  - a. Green Solder Mask Top
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<div><div>BADGER LOOP</div><div>Badgerloop ERB Room 133 1400 Engineering Drive Madison, WI 53706</div></div>	ENGINEER: Ryan Castle	TITLE:  lv_io_pcb.PcbDoc	
	PCB DESIGNER: Ryan Castle		
	DATE: 1/21/2019	PART NO.: 2019_03_A_1	REV: A
	FILE NAME: lv_io_pcb.PcbDoc	DWG NO:	SCALE: 1:1

