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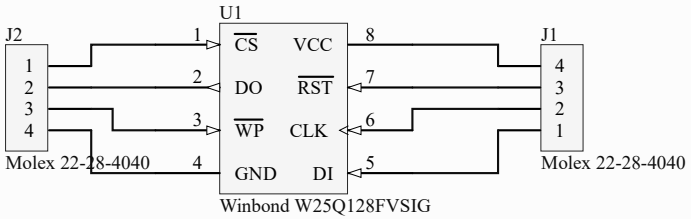

Title			
Size A	Number		Revision
Date:	12/26/2015	Sheet of	
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SOIC-8
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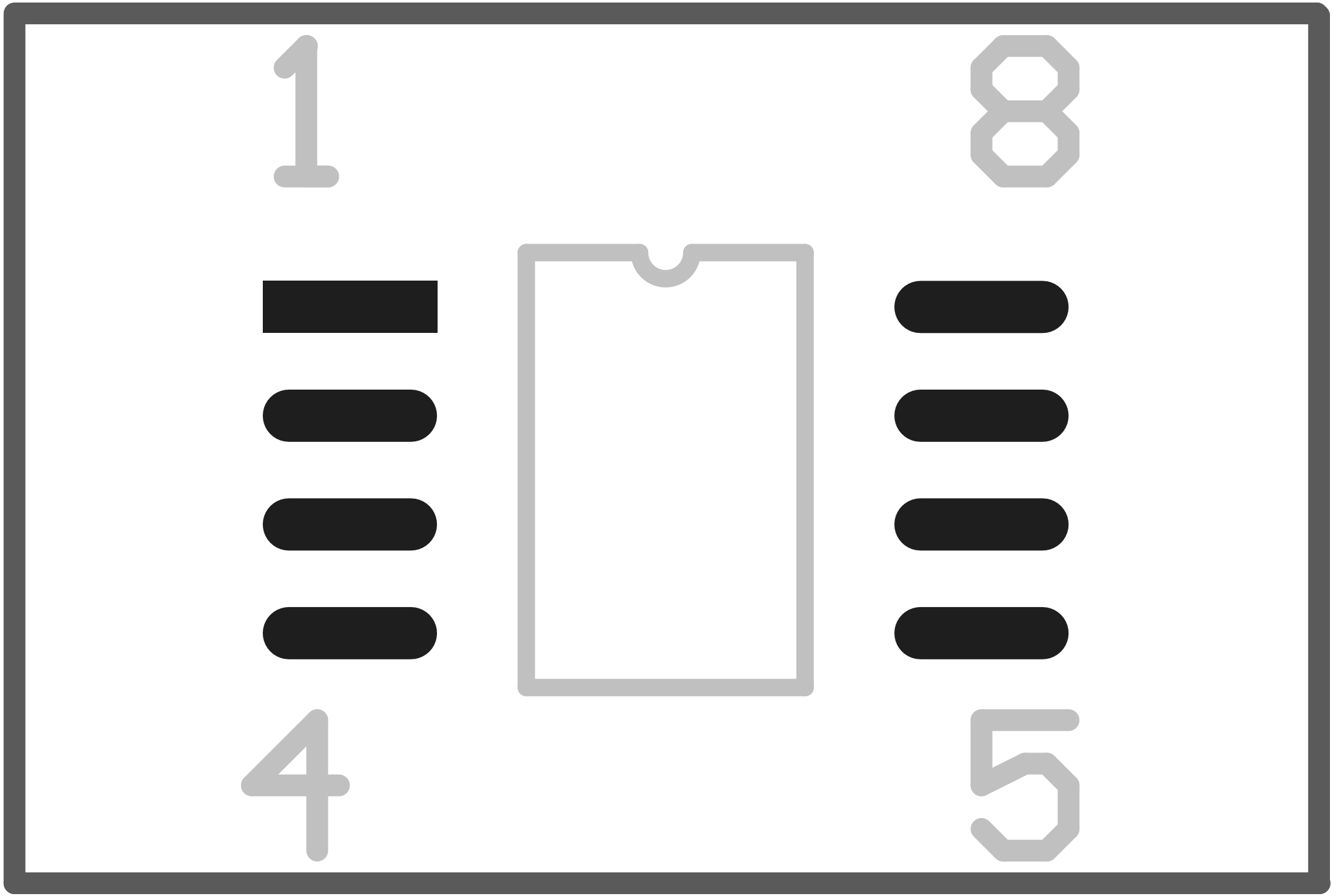
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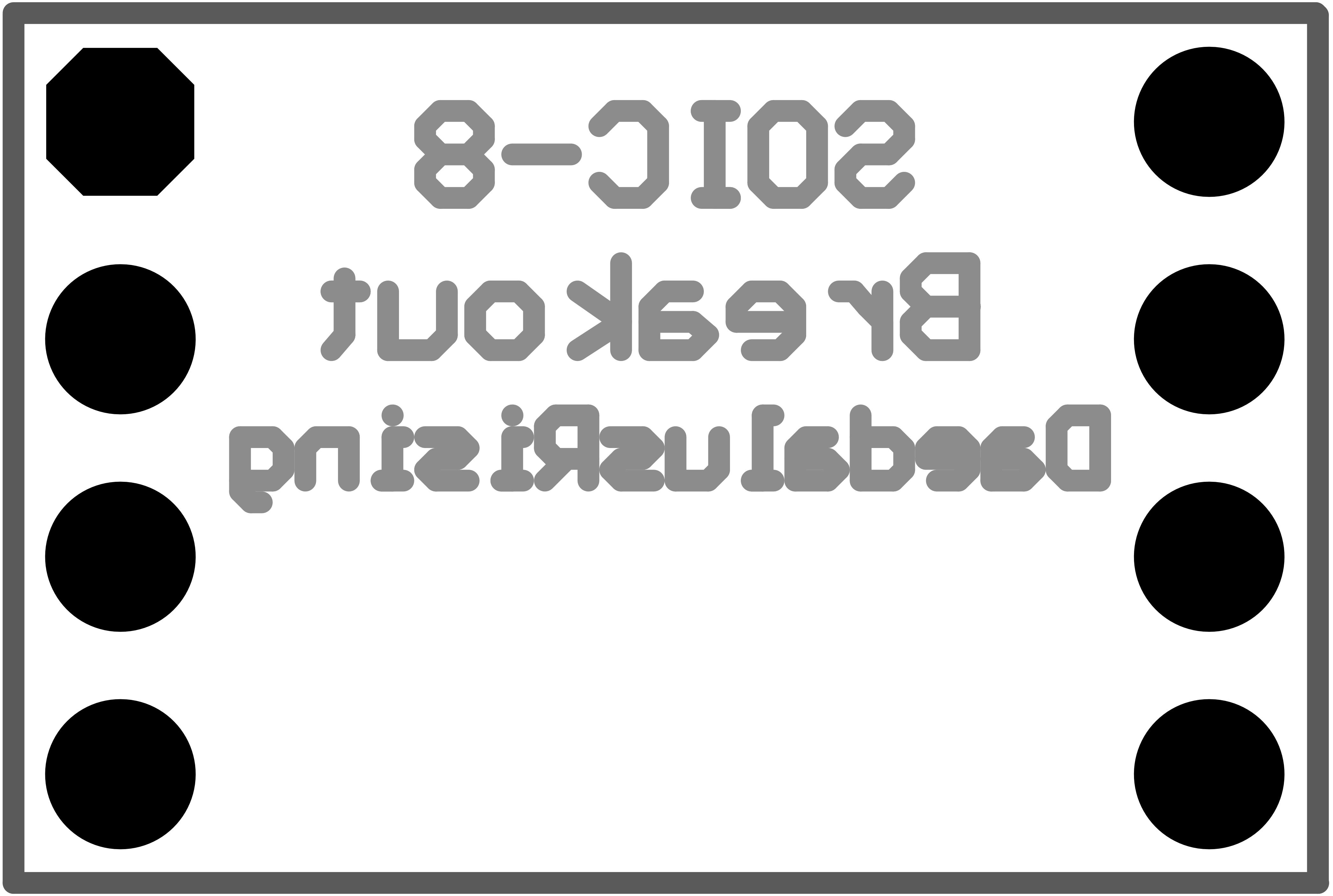
SOIC-8
Breakout
DaedalusRising

Design Rules Verification Report

Filename : C:\ProgramData\Altium\CircuitMaker {9AAAF7C6-4ED7-436D-B1BE-0297A78D81E8}\Projects\CCC25C86-F06C-4E03-A559-C43134DBC3E1\6a4fd9f3-8982-4cbc-bc18-111a2b153345\PCB1.CMPcbDoc

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Unpoured Polygon (Allow unpoured: False)	0
Net Antennae (Tolerance=0mil) (All)	0
Silk primitive without silk layer	0
Silk to Silk (Clearance=10mil) (All),(All)	0
Silk To Solder Mask (Clearance=10mil) (IsPad),(All)	0
Minimum Solder Mask Sliver (Gap=10mil) (All),(All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Hole Size Constraint (Min=1mil) (Max=100mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Width Constraint (Min=10mil) (Max=20mil) (Preferred=15mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Clearance Constraint (Gap=10mil) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Total	0

Electrical Rules Check Report

Class	Document	Message
		Successful Compile for SOIC-8 Breakout.PrjPcb